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SOUNDING ROCKET AIRBORNE PCM SYSTEM

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DECEMBER 1973

GSFC
GODDARD SPACE FLIGHT CENTER
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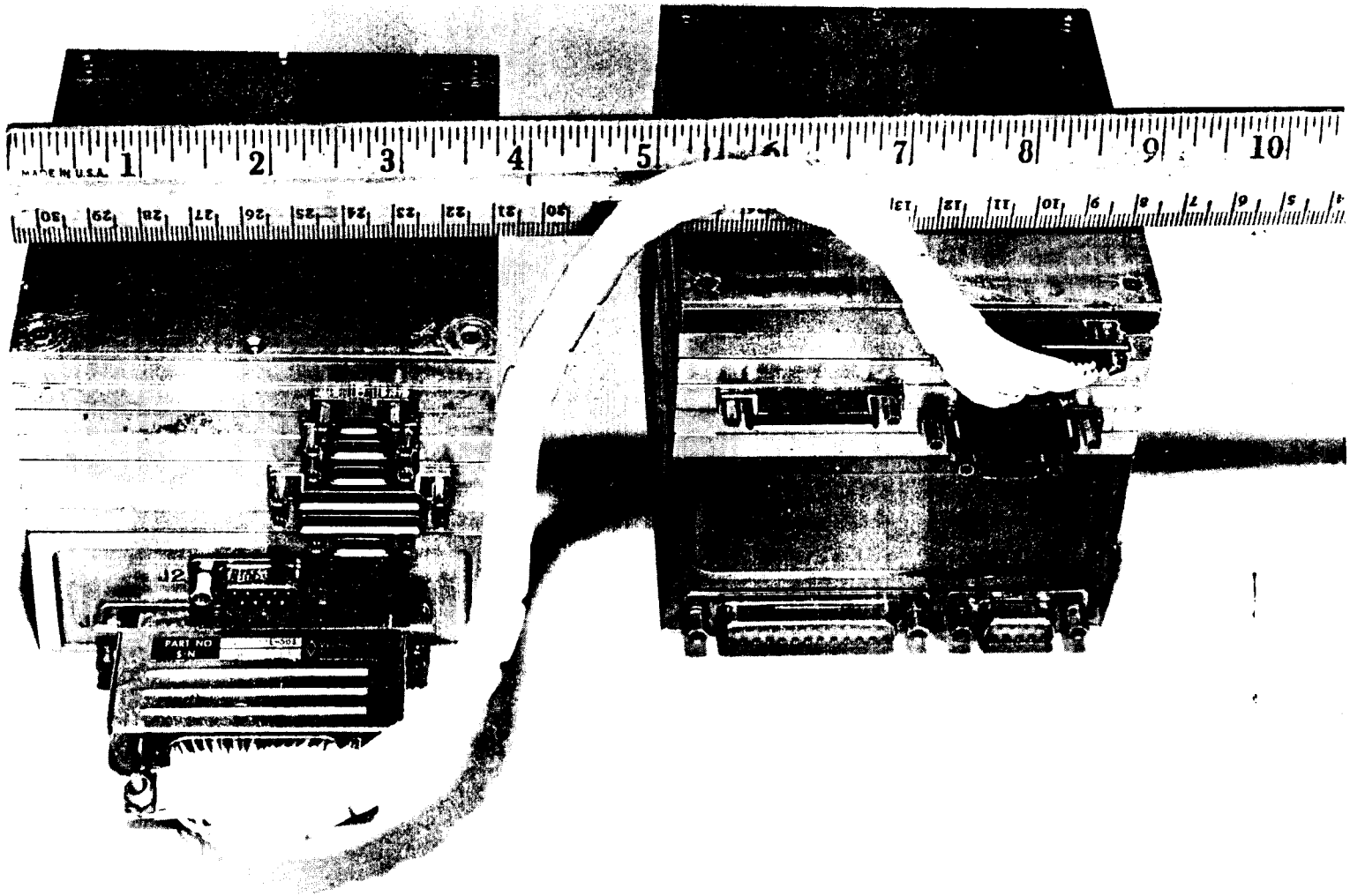
ABSTRACT

A flexible, low cost, self-contained, PCM encoder system capable of processing up to 448 data inputs is described. The modular construction of the system allows it to efficiently process a small number of analog inputs or be expanded in steps to handle a large variety of data including analog, serial, parallel and pulse inputs. The use of electronically programmed read-only memories yields a system that can be tailored to the experimenter's requirements without rewiring and can be responsive to last minute field changes, also without rewiring.



Frontispiece–A sample PCM system.

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INTRODUCTION

The PCM encoder here described was designed by the sounding rocket instrumentation section to meet the varied needs of sounding rocket experimenters. A general purpose mainframe encoder that can be used in conjunction with a number of special purpose expansion modules resulted in a PCM encoder system that is standardized to conserve turnaround time and cost, but which is easily tailored to any given requirements without any hardware rewiring being required.

A fully expanded encoder can process 448 different data inputs. The current inventory of expansion modules can handle analog, serial, parallel and pulse inputs. The physical and format expansion methods utilized allows the module inventory to be easily updated to meet future needs.

The use of AUGAT through terminals allows different types of modules to be arbitrarily stacked on top of the mainframe encoder (See Frontispiece). The number and type of expansion modules is determined by the experimenter's requirements. When the number of expansion modules is large enough to exceed the mainframe power supplies capabilities, a new stack of modules is started on top of a booster power supply.

The content of the data format generated by the mainframe encoder is automatically responsive to the number and type of expansion modules used (thus requiring no rewiring). This flexibility is accomplished by a priority structure and a common bus structure between the mainframe encoder and the expansion modules, a programmable address decoder on each module and the use of an electronically programmed read-only memory for complex data formats.

SUMMARY OF TERMS AND ABBREVIATIONS

A/D –	Analog to Digital
ADC –	Analog to Digital Converter
Bi-Ø-L –	Bi-Phase-Level
BPS –	(1) Bits per Second; (2) Booster Power Supply

D/A –	Digital to Analog
DAC –	Digital to Analog Converter
LSB –	Least Significant Bit
Mainframe –	Columns of a format (See Figure 2)
MOS –	Metal - Oxide - Semiconductor
MSB –	Most Significant Bit
PCM –	Pulse Code Modulation
PROM –	Programmable Read Only Memory
Subcommutate –	Data Sampling at rates which are Submultiples of the Subframe Rate
Subframe –	Rows of a Format (See Figure 2)
Super commutate –	(1) Data Sampling at Rates which are Multiples of the Subframe Rate (super-commutating a submodule)
	(2) Data Sampling at Rates which are Multiples of the mainframe rate (super-commutating a mainframe channel)

FUNCTIONAL DESCRIPTION

General Operation

The PCM encoder (Figure 1) accepts experimenter's inputs through the mainframe encoder's 14-channel analog multiplexer or through the expansion modules. Analog data is multiplexed onto a common analog bus and converted to 9 bit parallel digital information during the word preceding its entry into the PCM output. Serial digital information is also processed (shifted in) during the word preceding its entry into the output. Pulse count and parallel data do not need advance processing.

The A/D converter, the sync code generator, and each channel of the digital modules have a data transfer gate through which they gain access to the parallel PCM data bus. The selected gate is opened and its contents are loaded into the output register during the time that the output logic is generating the parity bit of the previous word.

The clock, timing and address lines generated by the control logic are distributed throughout the mainframe encoder. If expansion modules are used, the clock and timing information is applied to them. The address lines may be used directly by the expansion modules or converted to any arbitrary address by a programmable address converter prior to being distributed to the expansion modules. If a large number of expansion modules are used, a booster power supply is utilized to augment the mainframe power supply.

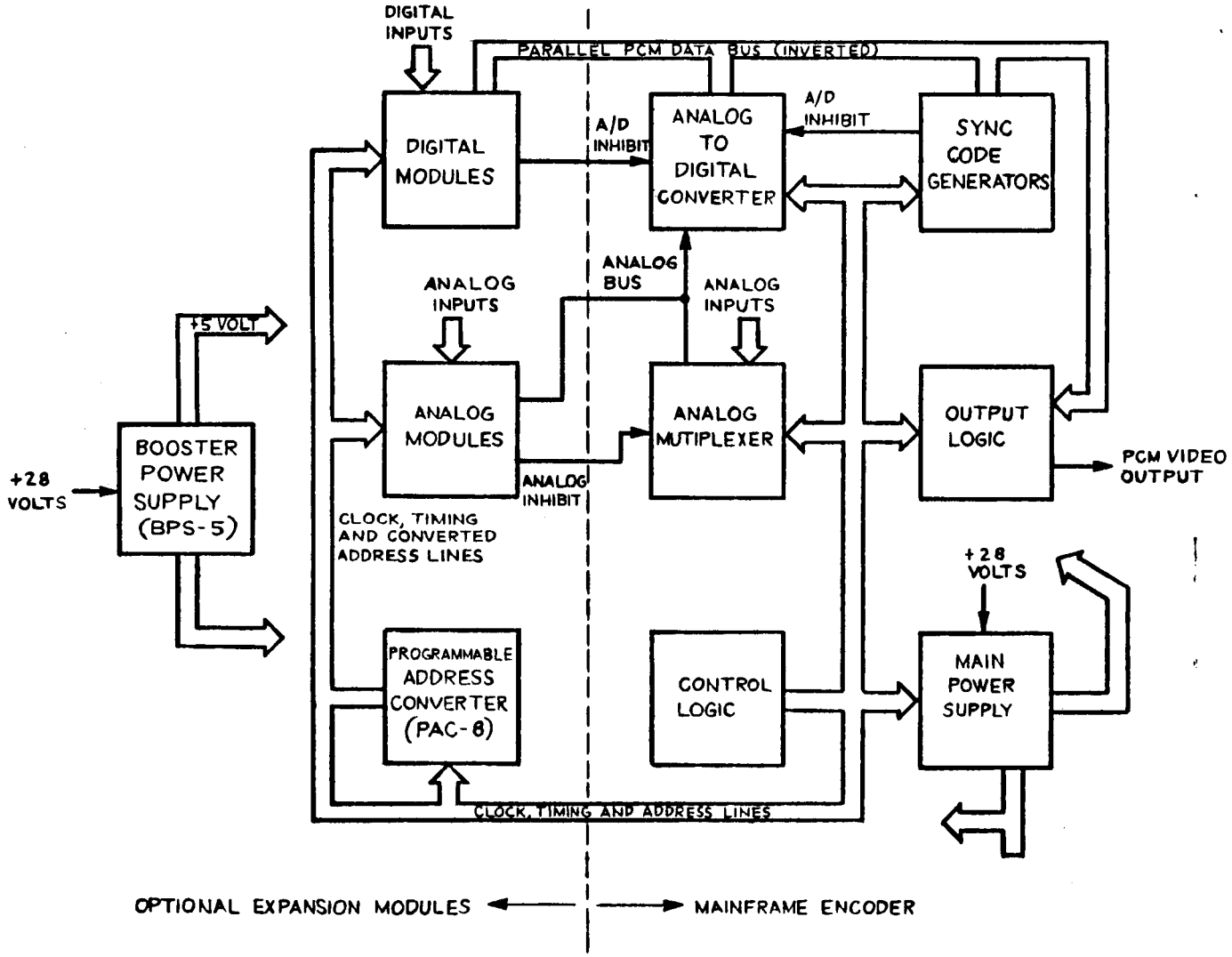


Figure 1. PCM system block diagram.

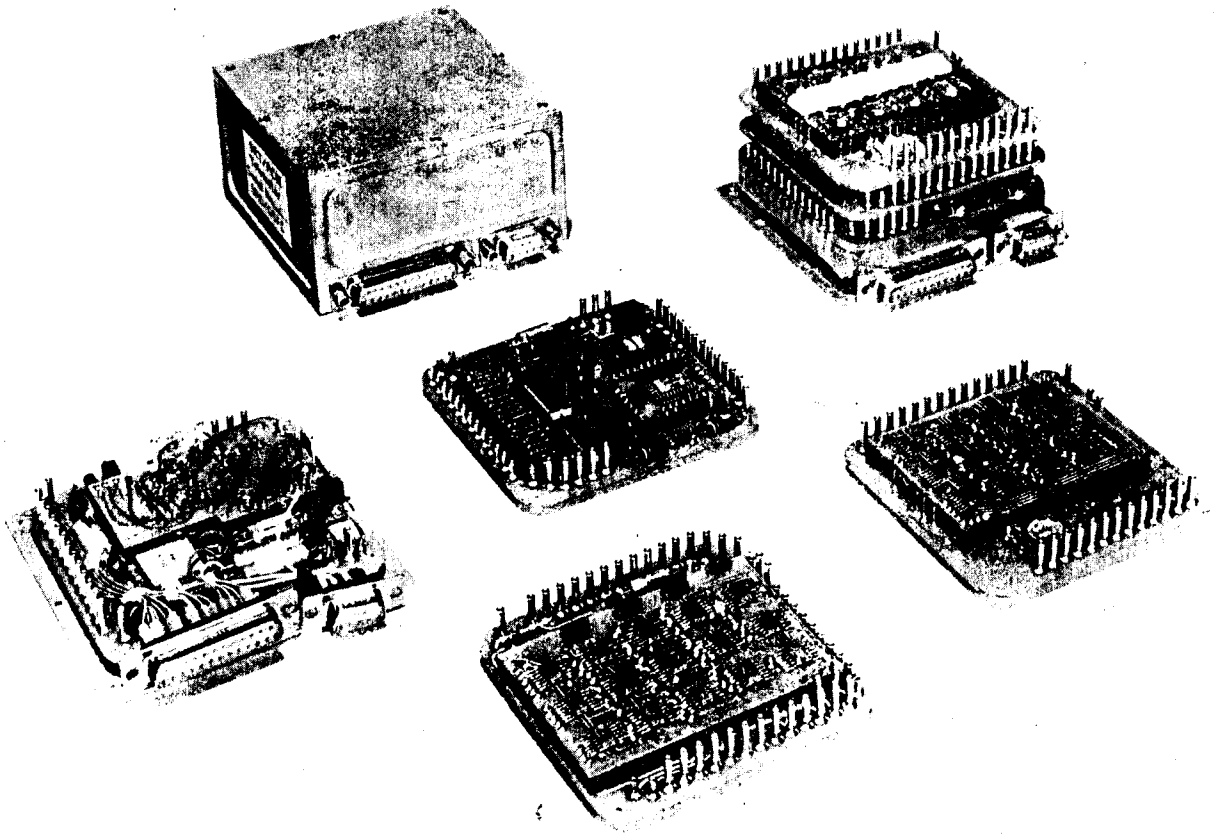


Figure 2a. Mainframe encoder (several views).

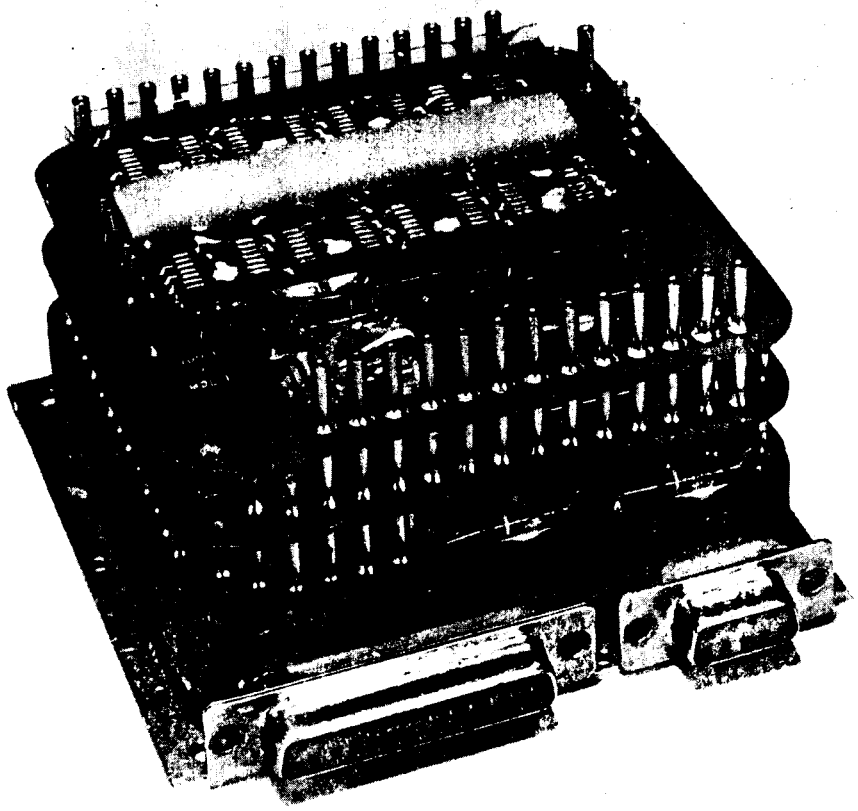


Figure 2b. Mainframe encoder (closeup).

Mainframe Encoder

The mainframe encoder consists of the following six functional parts: (Figure 2.)

1. Control Logic	Generates a 512 word format and all required timing signals (Figure 3).
2. Sync Code Generator	Generates a 14 bit sync code and multiplexes this sync code along with the 5 bit subframe address into the first two mainframe channels.
3. Analog Multiplexer	Multiplexes one of the 14 mainframe analog inputs at a time into the A/D converter.
4. Analog to Digital Converter	Converts all analog inputs into a 9 bit digital word.
5. Output Logic	Converts the 9 bit parallel PCM data bus into a 10 bit, filtered, Bi-Ø-L serial output with odd parity (MSB FIRST, PARITY LAST).
6. Power Supply	Generates all the power requirements for the mainframe encoder and a number of expansion modules (See Appendix A) from a 28 volt DC input.

Control Logic

The control logic section of the mainframe encoder generates the clock signals, timing signals and address lines required by the rest of the system. (See Figures 4 and 5.)

The output of a 4MHz crystal oscillator is divided by 10, 2 and 10 to generate a 400KHz A/D clock, 200KHz bit clock and 20KHz word clock respectively. The word clock drives a 4-bit counter to generate the mainframe address lines which in turn drives a 5-bit counter to generate the subframe address lines.

An array of gates within the timing logic block generates the required timing signals during each word. The data transfer signal is used to strobe digital information onto the parallel PCM data bus for loading into the output shift register. The data reset signal is an auxillary signal used by certain expansion modules; the RCM-4 module uses the data reset signal to reset counters after their contents have been read out. The parity reset signal is used by the output logic to reset the parity flip-flop in preparation for the next word. The A/D converter start signal resets and then starts the analog to digital converter.

Sync Code Generator

The Sync Code Generator section of the mainframe encoder generates the PCM sync code during mainframes 0 and 1. The sync code consists of a 14-bit autocorrellation code, a 5-bit subframe address and a parity bit as shown on page 9.

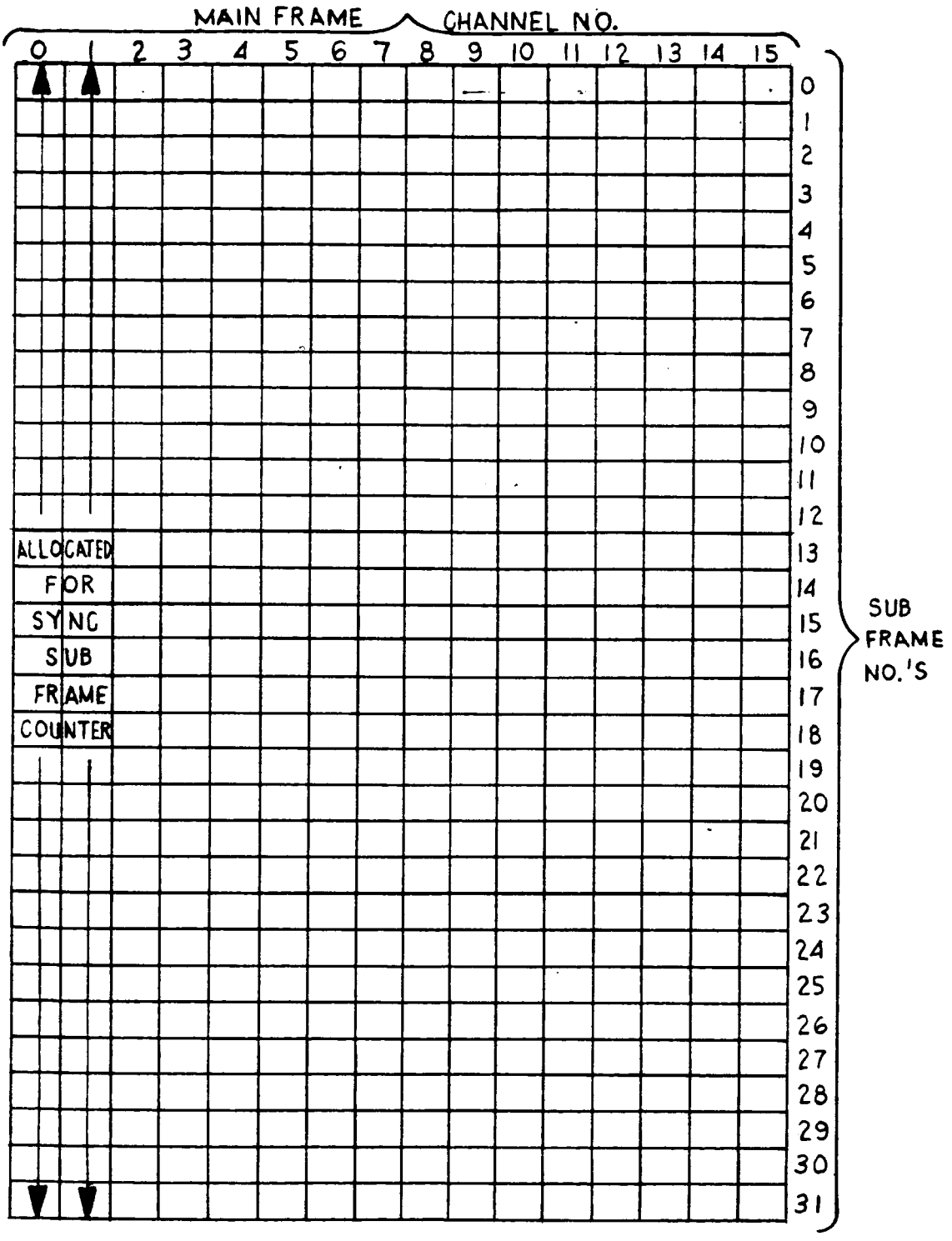


Figure 3. Data matrix.

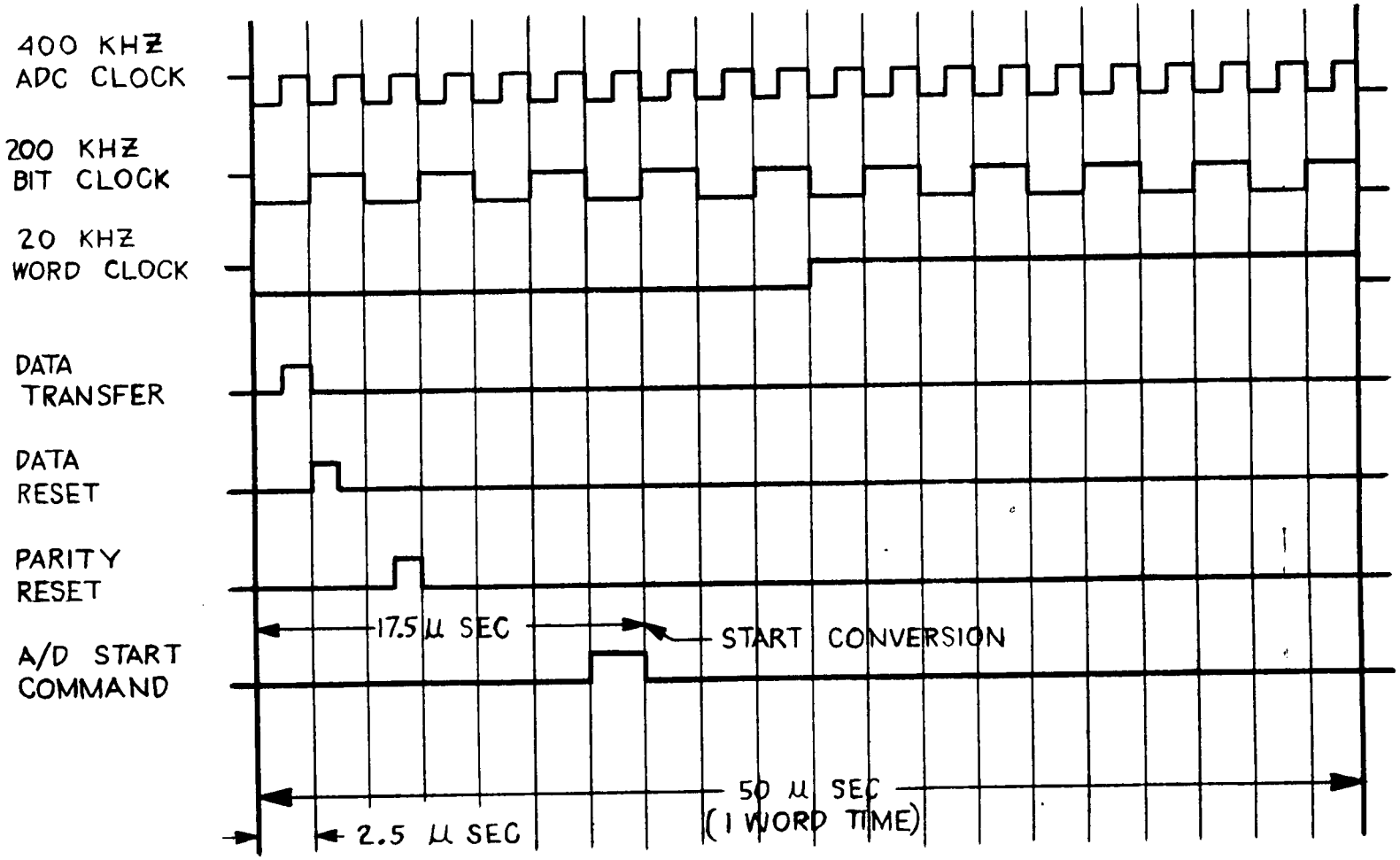


Figure 4. Mainframe encoder timing diagram.

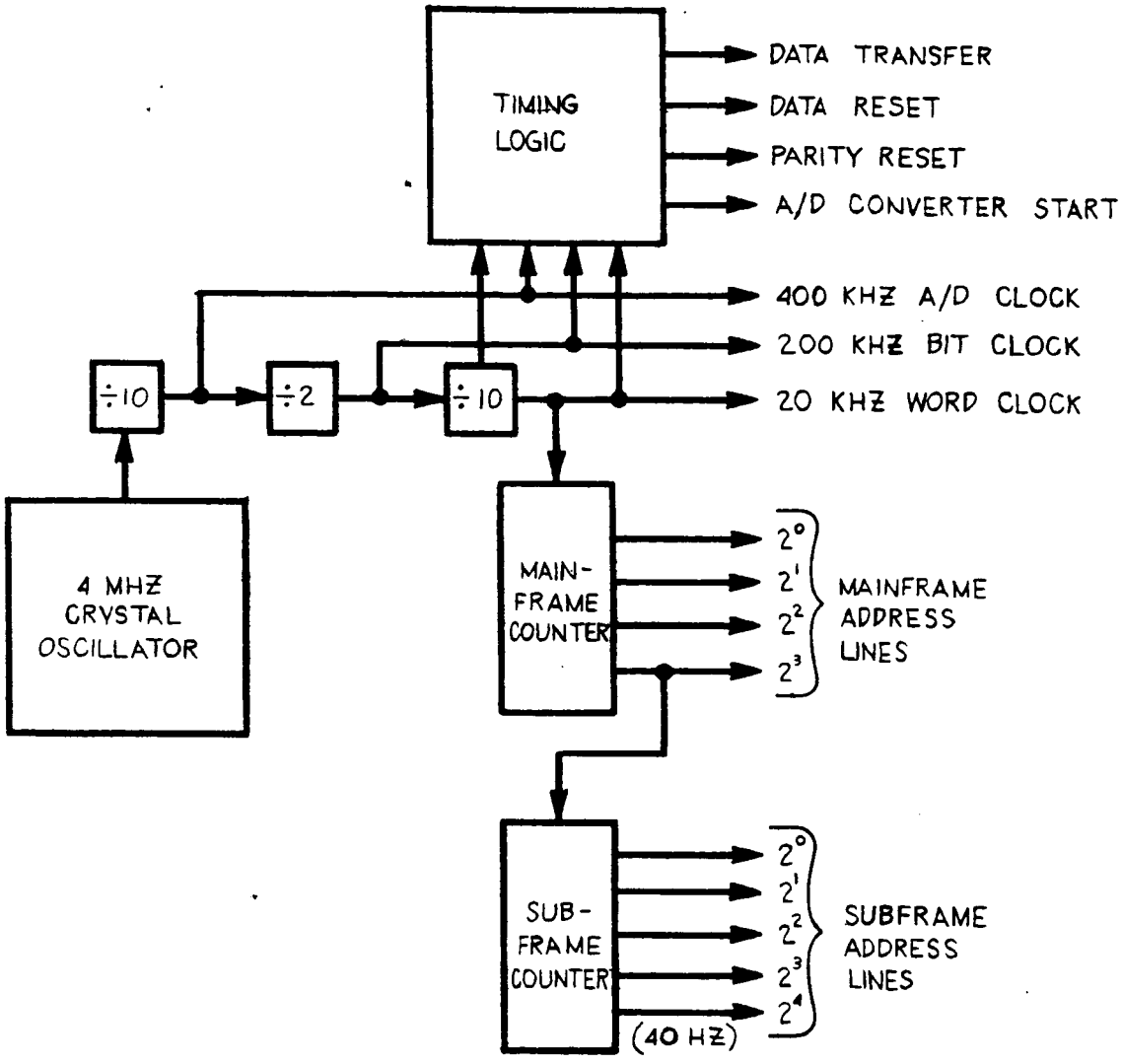


Figure 5. Control logic block diagram.

Word 0

1 0 0 1 1 0 0 1 0 1*

MSB LSB

Word 1

1 1 1 1 2^0 2^1 2^2 2^3 2^4 p*

MSB Subframe Address LSB

*Generated by parity logic.

The mainframe address lines are decoded into frame 0 and frame 1 sync select lines. (See Figure 6.) During the data transfer time, these lines select the appropriate data transfer gate to place the sync code on the parallel PCM data bus. The sync select lines are also OR'ed to form an A/D inhibit line.

The LSB of all words is followed by the odd parity bit. In the case of word 0, the nine data bits are fixed and hence the parity bit is always 1 and can be considered as one of the 14 fixed, sync code bits.

Analog Multiplexer

The analog multiplexer section of the mainframe encoder allows analog data to be multiplexed into any of the 14 mainframe data channels. (See Figure 7.) An input protection circuit consisting of diode clamps and a series resistor for each channel guards the MOS multiplexers from over or reverse voltages, up to ±35 VDC.

Since the mainframe multiplexer is not capable of subcommutation, an analog inhibit input is provided that disables the multiplexer. This inhibit is generated by one of the analog expansion modules (See AS-32 or ASC-32) which then multiplex their inputs onto the analog bus, at subframe rates.

The analog inputs are multiplexed at the beginning of the frame preceding their location in the format. This 50 microsecond word time is needed to allow the analog data to settle and to convert it to digital information.

Analog to Digital Converter

The analog to digital converter section of the mainframe encoder is a 9-bit, successive approximation A/D converter. (See Figure 8.) The A/D start command is issued 15 microseconds after the word boundary. (See Figure 5.) During the 2.5 microsecond duration of the command, the converter's timing and storage sections are reset. The conversion begins at the end of this command. During the 17.5 microseconds between the word boundary and the beginning of the conversion, the selected analog input is multiplexed onto the analog bus and allowed to settle.

The conversion takes place MSB first at a clock rate of 400 KHz. Initially the timing control circuitry forces the MSB storage register to a "1" and the 8 LSB registers to "0". The switch/ladder/reference network is configured as a digital to analog converter (DAC). The mid-scale DAC output is compared to the analog bus input. If the input is less than mid-scale, the MSB is reset to "0". If the input is greater than mid-scale, the MSB is retained as a "1". The timing control circuitry then forces successively lower order bits to "1's" and resets or retains them if the input is less or greater than the DAC output respectively. The total conversion takes 9 clock periods (22.5 microseconds).

2.5 microseconds after the next word boundary the contents of the storage register are strobed onto the parallel PCM data bus through the data transfer gate unless the A/D

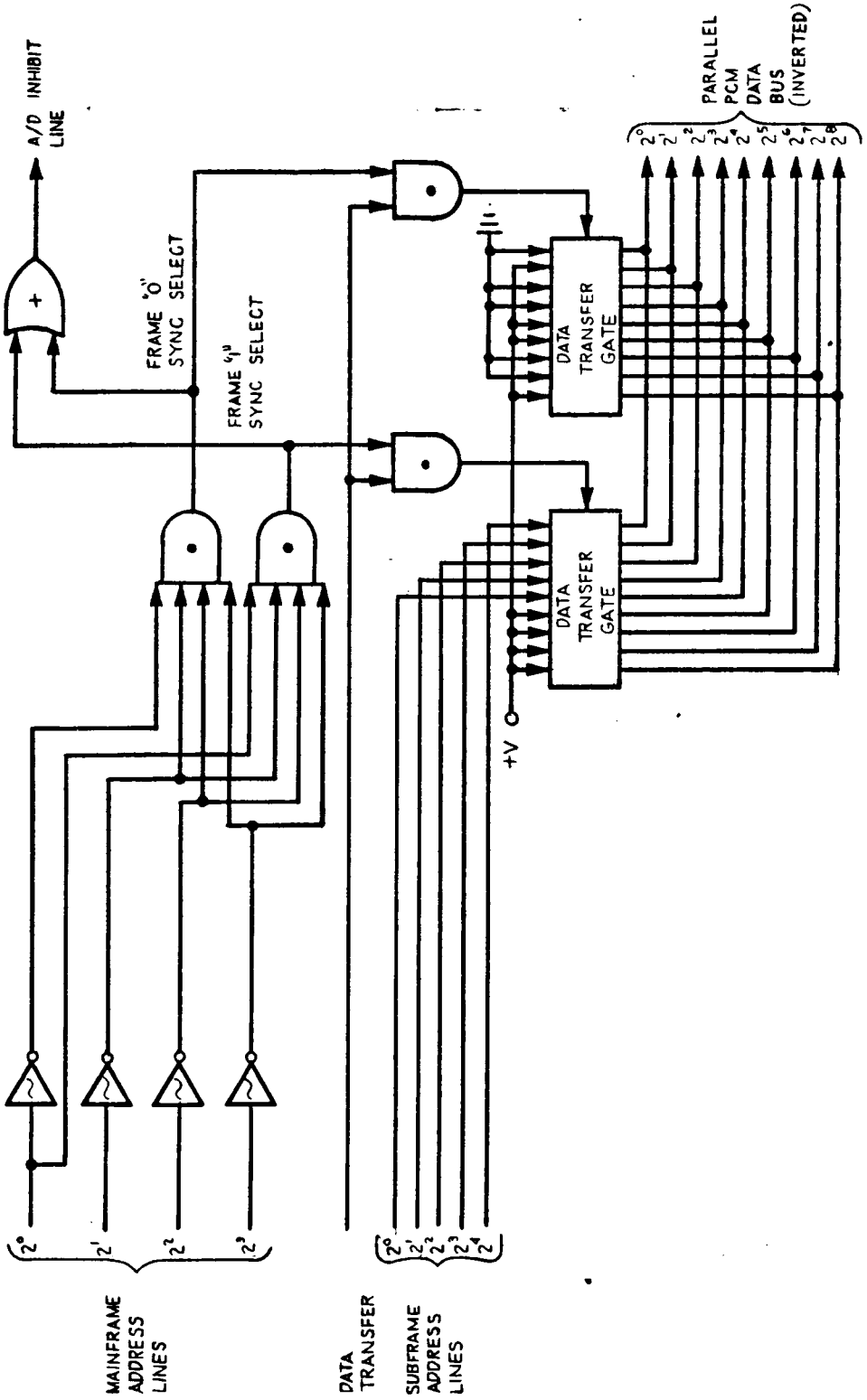


Figure 6. Sync code generator block diagram.

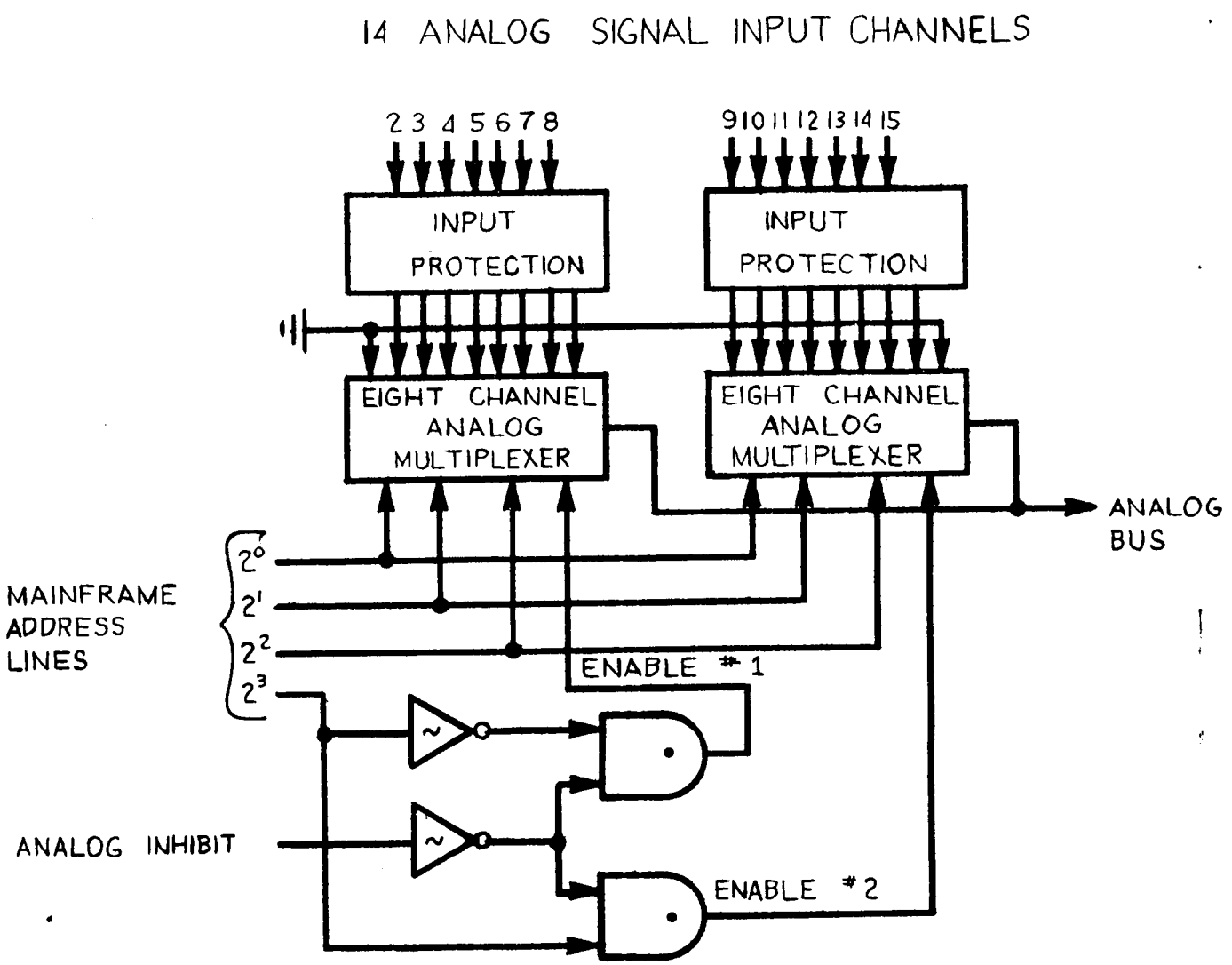


Figure 7. Analog multiplexer block diagram.

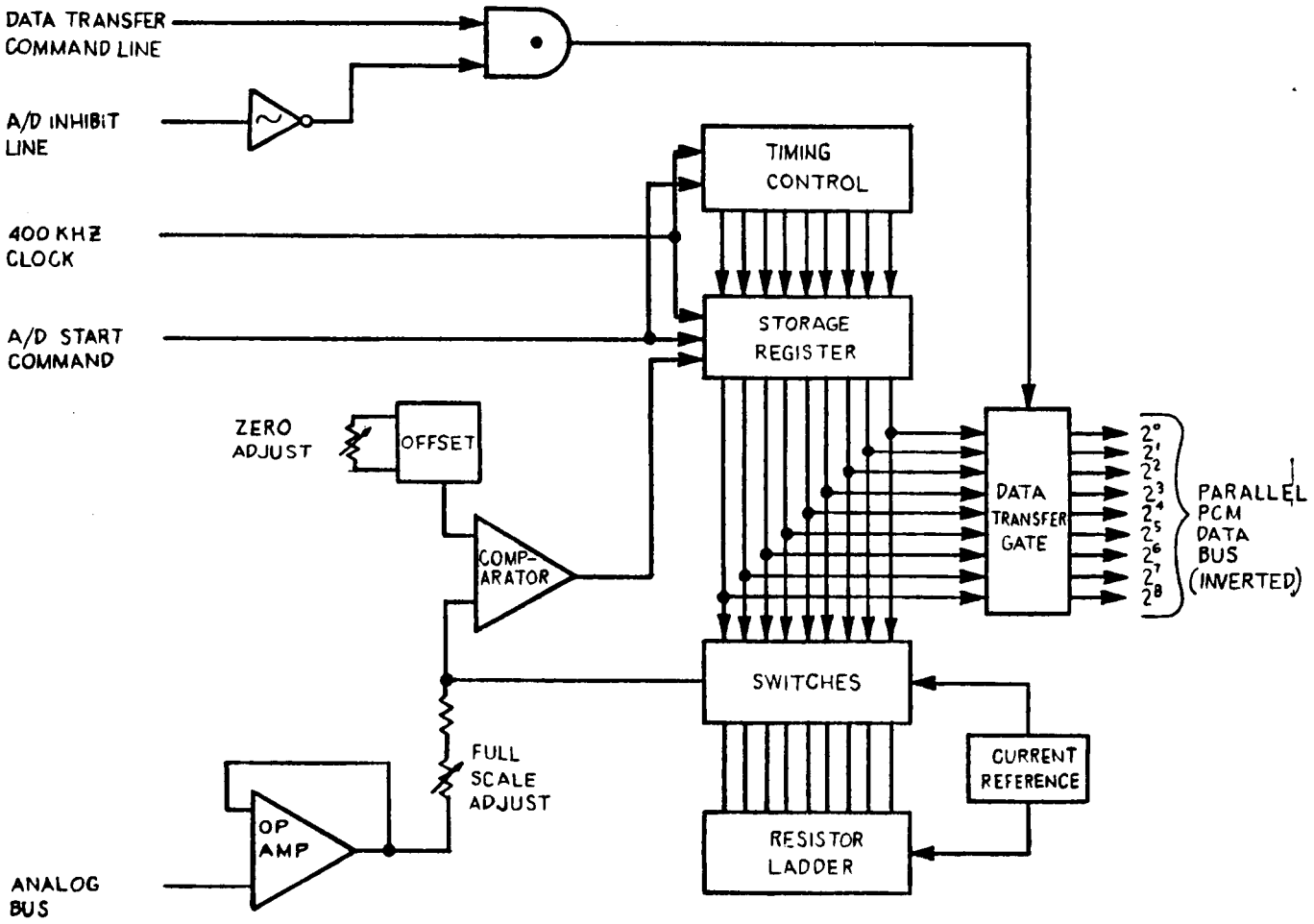


Figure 8. Analog to digital converter block diagram.

inhibit line is true. A true inhibit line indicates that digital information is taking precedence over the converted analog information. (See priority section.)

Output Logic

The output logic section of the mainframe encoder converts the 9-bit parallel PCM data bus into a 10-bit filtered, Bi-ϕ-L serial output with odd parity. (See Figure 9.)

The inverted PCM data is shifted out MSB first at 200 K BPS. The output is taken off the $\overline{Q}$ output of the last shift register to correct the polarity of the data. During the shifting process, the parity flip-flop records "1" if an even number of "1's" have been shifted out and a "0" if an odd number have been shifted out.

On the 9th shift pulse, the parity bit decoder disables the shift register and multiplexes the binary output from the shift register to the parity flip-flop for one bit time. During this time, the selected data transfer gate strobes the inverted parallel PCM data for the next word onto the bus. Since "1's" have been shifted into the register during the shifting out of the previous word, "0" inputs reset the register and "1's" leave the register in their set position. At the end of the parity bit time, the binary output is multiplexed back to the data and the parity bit is reset.

The binary output is then exclusively OR'ed with the bit clock which results in each bit being inverted for the last half of the bit time thus yielding a bi-phase-level (Bi-ϕ-L) output code.

The output is then bandwidth limited in a maximum-linear-phase premodulation filter.

Power Supply

The power supply section of the mainframe encoder converts the 28 volt DC input supply to the +5 volt, +12 volt, -12 volt and -27 volt supplies required by the mainframe encoder and expansion modules. (See Figure 10.)

Initially, the control module supplies a free running clock to the synchronous chopper. When the control logic section begins generating clock signals, the control module shifts from its internal clock to the 20 KHz system clock to increase the power supply efficiency. This process will automatically reverse if the system clock fails. The 20 KHz clock signal is divided by 2 and both polarities are applied to the chopper.

The hybrid voltage regulator senses the +5 volt line. The other outputs are slaved to +5 volts. Transient protection is provided by supressor diode CR1.

Bridge rectifiers and capacitive filters are used on each output. The power supply is capable of sustaining a short circuit for 30 seconds without permanent damage.

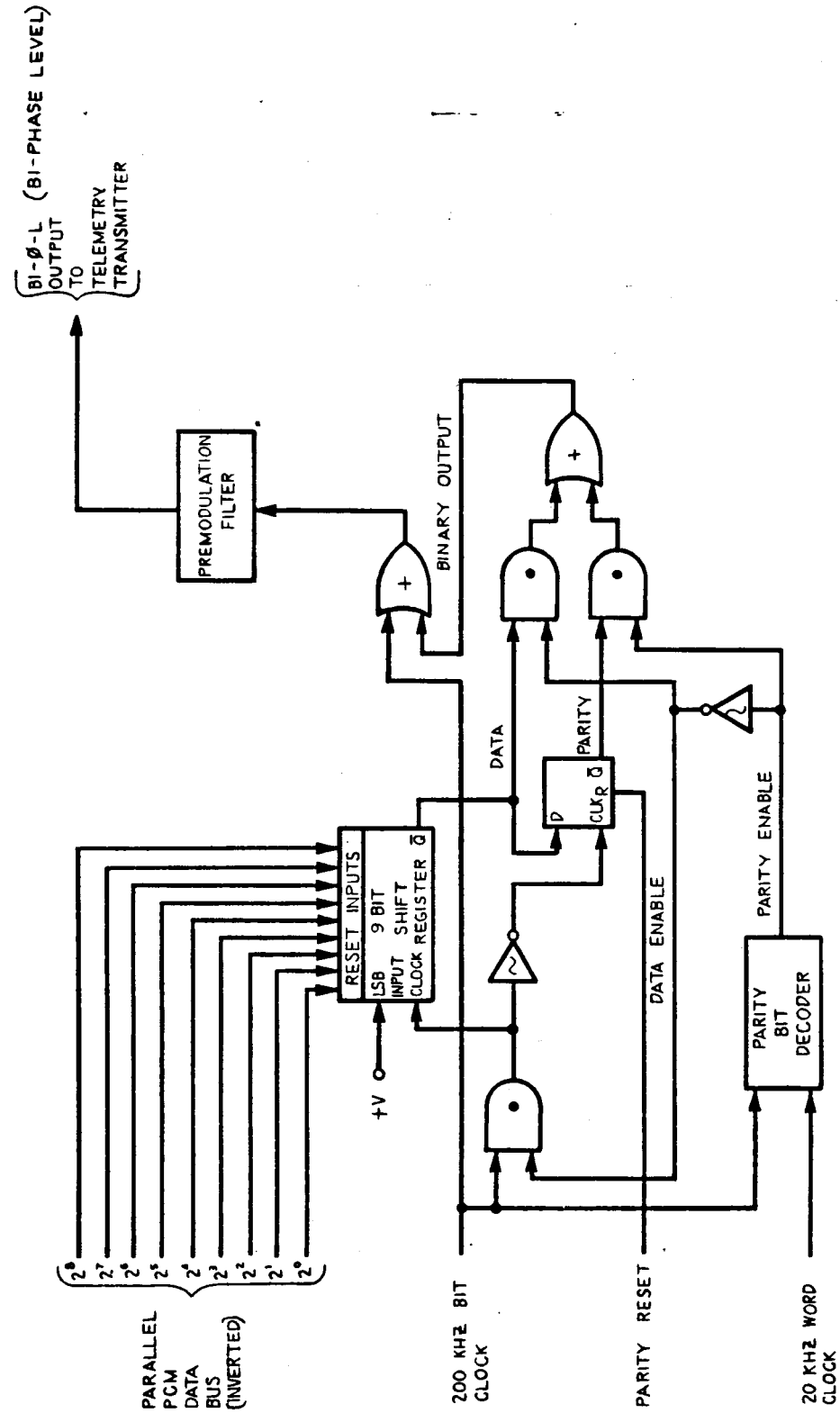


Figure 9. Output logic block diagram.

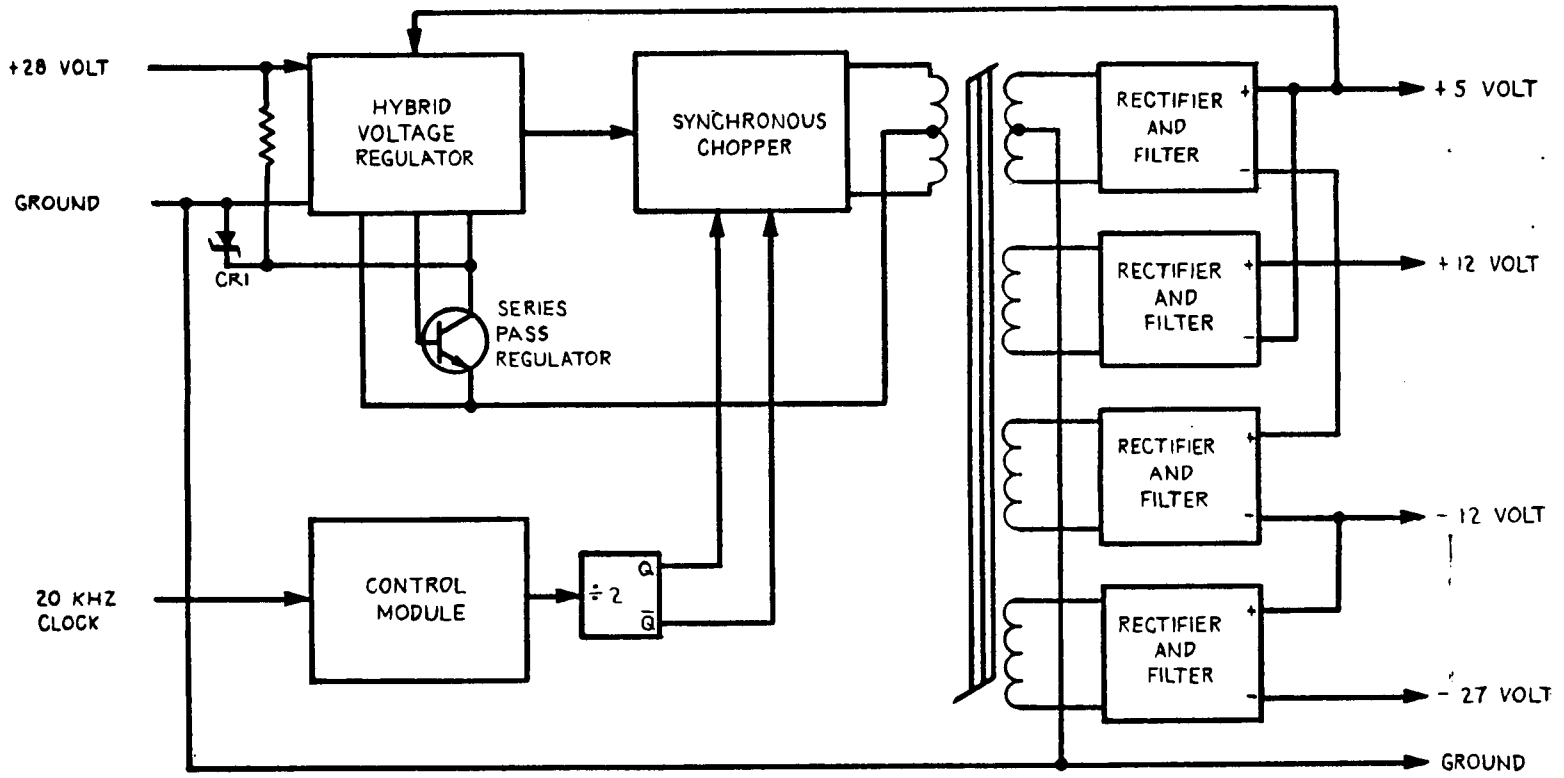


Figure 10. Power supply block diagram.

Expansion

Any or all of the 14 mainframe analog channels of the mainframe encoder can be expanded to include up to 32 data sources each, for a total of 14 x 32 = 448 data sources for the entire system. These data sources can be analog, digital or any combination of analog and digital, but digital data can only be multiplexed up to 16 levels per mainframe channel, while analog signals can be multiplexed up to 32 inputs per mainframe channel. Details of the various expansion modules are given in sections following this one.

Priority

A priority arrangement within the mainframe encoder allows the expansion modules to override the 14 mainframe analog channels. The highest priority is given to digital data. This is accomplished by inhibiting the A/D data transfer gate during the data transfer time. Each digital module produces an A/D INHIBIT signal during the time it is strobing data onto the parallel PCM data bus.

The next highest priority is given to subcommutated analog data. This is accomplished by inhibiting the mainframe analog multiplexer and replacing its output with a subcommutated analog output. Each analog module produces an ANALOG INHIBIT signal and has its analog data output tied into the analog bus. If neither an A/D INHIBIT nor an ANALOG INHIBIT is generated, the mainframe analog data will be processed.

Programmable Address Decoder

Each digital expansion module contains a programmable address decoder. (The analog expansion module decoder is explained in the AS-32 section.) Within the decoder, an array of jumpers is used to program the desired mainframe(s) and subcom degree for the 4 digital circuits in each module. A list of jumper configurations and an explanation of the programming nomenclature used is contained in Appendix A.

Because of the wide variety of programming requirements needed to meet all Sounding Rocket experiments, a scheme had to be devised to eliminate the need to program modules specifically for a particular experiment. This is accomplished by use of the PAC-8 module which converts address lines from the mainframe encoder to any arbitrary set of new addresses. By using the PAC-8, it is possible to stock modules which have arbitrary hardwire programming and then use the PAC-8 to convert them to any required configuration without having to rewire the module address decoder. (See PAC-8 section for details.)

Programmable Address Converter (PAC-8)

The programmable address converter (PAC-8) is a 2048 bit, electronically programmable read-only memory (PROM). It is configured as a 256 word by 8 bit array and is erasable by the application of ultra-violet light and reprogrammable by a computer-based programmer. (See Figures 11 and 12.)

Figure 11. Programmable address converter (PAC–8).

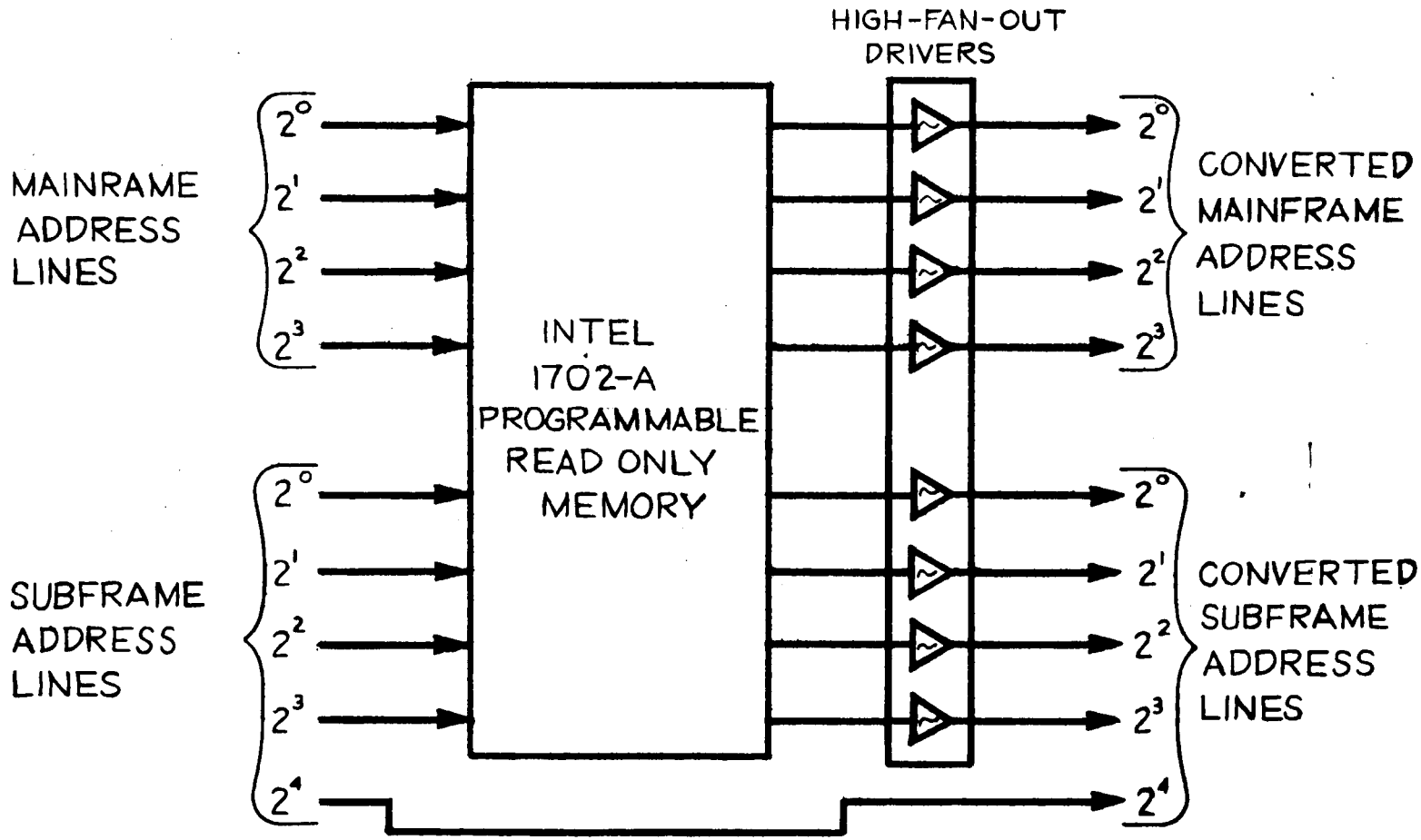


Figure 12. Programmable address converter block diagram.

The mainframe address and the four LSB's of the subframe address lines address the PROM. The eight bit output becomes the new address information. Therefore, with the exception of the subframe MSB, any address can be arbitrarily transformed into a different address. The programmable address decoders in each type of expansion module now only need to be programmed for a unique mainframe and subcom degree and any data format can be constructed.

An additional benefit of the PROM is that the entire program can be erased and a new program stored in the field within a few hours with no rewiring required.

Analog Submultiplexer Module (AS-32)

The analog submultiplexer (AS-32) is used to multiplex up to 32 analog data signals onto the analog bus. (See Figures 13 and 14.) The AS-32 consists of four 8-channel MOS multiplexers that are controlled by two address decoders. Each analog input channel is protected with a diode clamp circuit that provides both reverse and overvoltage protection up to 35 VDC.

The mainframe address lines are decoded into sixteen mainframe select lines. The proper select line is connected to the one out of four decoders by a jumper. Since the A/D conversion takes place one frame prior to outputting, the proper decoder output number is one frame number less than that specified. Therefore, when an analog input is to be outputted during mainframe X, it must be submultiplexed and converted during mainframe X-1. If, for example, it is desired to utilize an AS-32 during mainframe 2, then the programming jumper would be placed on the mainframe decoder output corresponding to mainframe 1 as shown.

The subframe address lines are decoded in a straightforward manner; the two MSB's are decoded and select one of the four-eight channel analog signal multiplexers, and three LSB's are applied to directly to all four of the analog signal multiplexers.

The analog signal output from each of the four MOS multiplexers are connected together to form a common analog BUS that is routed to the ADC in the mainframe encoder. When an analog input is selected, an analog inhibit signal is generated that disables the mainframe analog multiplexer.

Analog Submultiplexer with Calibrator and Bi-Level Monitor (ASC-32)

The Analog Submultiplexer with Calibrator and Bi-Level Monitor (ASC-32) is used to expand a single mainframe channel to 32 submultiplexed channels. The 32 submultiplexed channels consists of 30 analog submultiplexed channels, a submultiplexed channel that contains a precision voltage calibrator, and a channel that provides nine, 1-bit word monitors. The sampling rate for each of the 32 channels is approximately 40 Hz.

The ASC-32 consists of two circuit boards one of which (A1) contains the 32 channel submultiplexer. The second board (A2) contains the precision calibrator and bi-level monitor

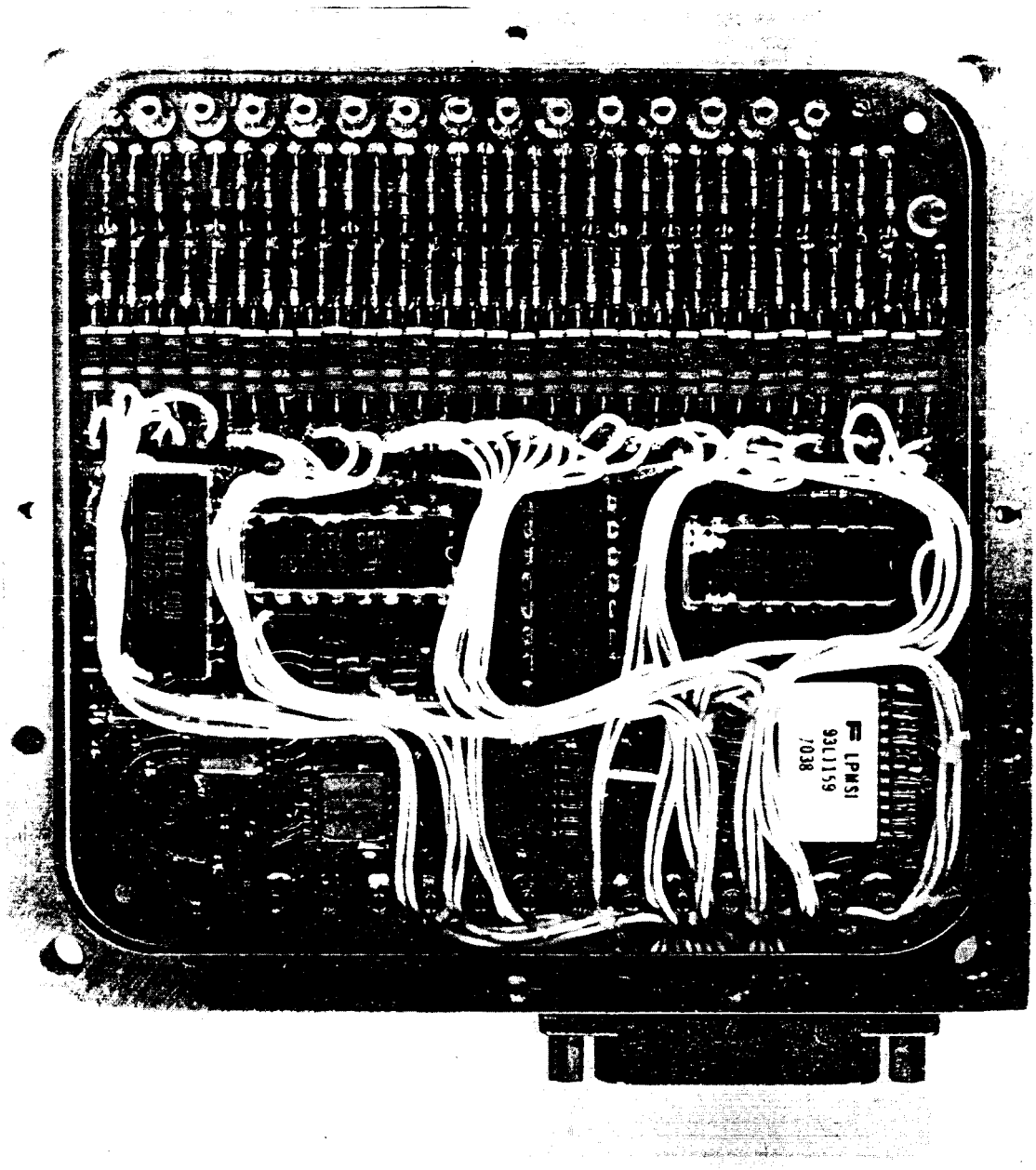


Figure 13. Analog submultiplexer (AS-32).

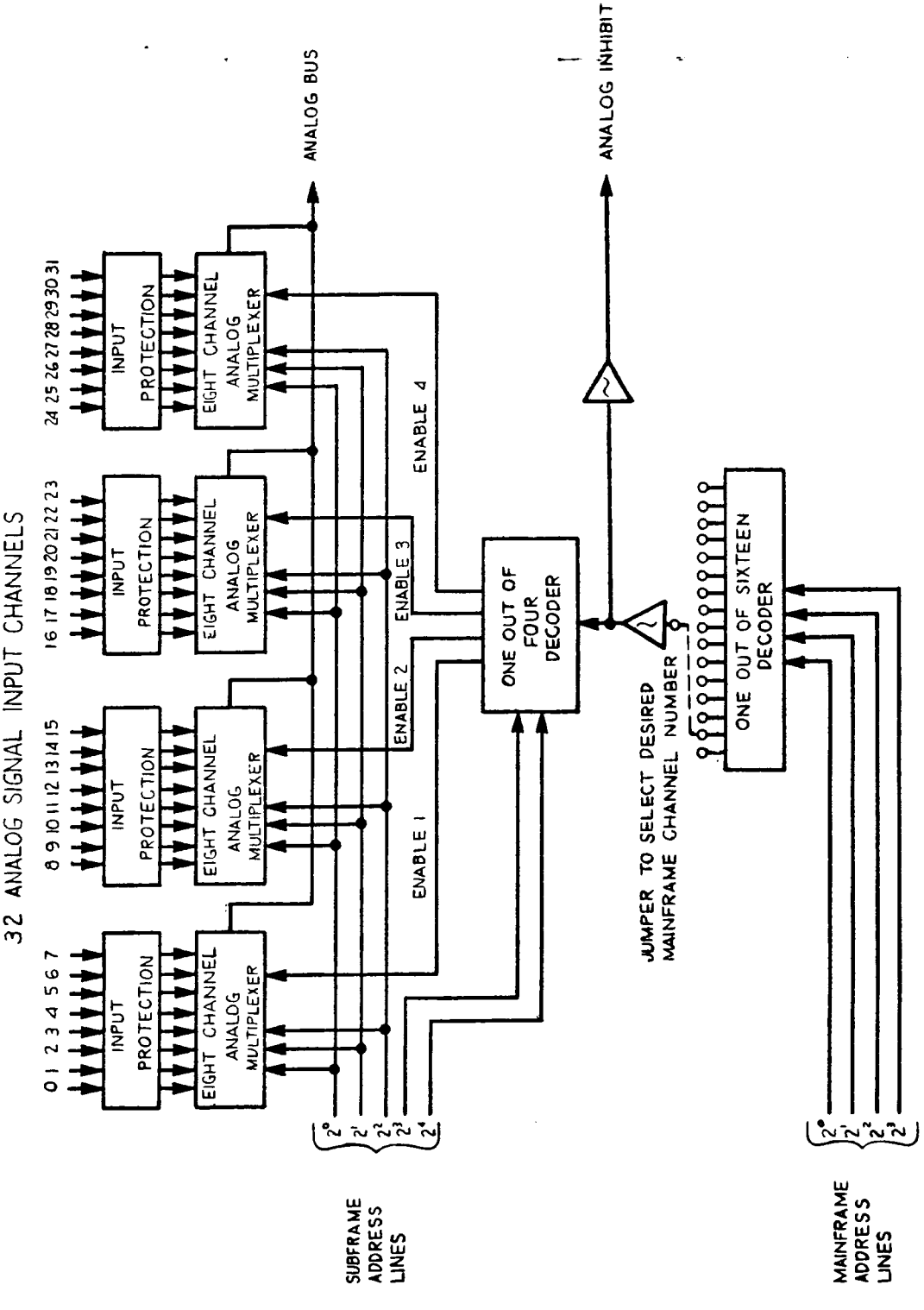


Figure 14. Analog submultiplexer block diagram.

function. (See Figures 15 and 16.) Board A1 is identical to the Analog Submultiplexer module (AS-32) in all aspects except that subframe 0 is reserved for outputting the bi-level monitor information and subframe 31 is reserved for the inclusion of the calibration information.

The calibrator on board A2 consists of a zener voltage reference supply and amplifier, a precision resistor divider network, an eight channel multiplexer, a module eight counter, and a buffer amplifier. The bi-level monitor function consists of a subframe 0 detector and a nine bit data input protection circuit followed by a 9-bit transfer gate. The five subframe address lines are first buffered and then AND'ed together with the logic signal that determines the mainframe channel in which the bi-level monitor information is to appear. The output of the AND gate will be true only in subframe 0. The output of this AND is also used to inhibit the operation of the A/D converter in the main encoder (A/D Inhibit output line).

The enabling logic level for the data transfer gates is the AND of the subframe 0 detector and the data transfer signal from the main encoder. The nine bits of bi-level information are then strobed onto the parallel PCM data bus at the proper time in subframe 0.

The calibrator reference voltage is obtained from a zener supply that is the input to a fully compensated inverting amplifier with a gain of less than one. The +5.0 reference voltage output of the amplifier is divided down into +4.0, +3.0, +2.0, and +1.0 volt levels by a precision resistor network. The five reference voltages along with one analog ground reference are then multiplexed into subframe 31 of the selected mainframe channel. The divide-by-eight counter which steps the multiplexer is driven from the MSB of the subframe address; the sequence of reference voltages is: +5.0v, +4.0v, +3.0v, +2.0v, +1.0v, 0v, 0v, and 0v. These reference voltages from the multiplexer are first buffered by a non-inverting amplifier in the follower configuration prior to being submultiplexed in subframe 31. The buffer amplifier has a zero volt adjustment for precise control of the calibration voltages.

Counter Module (RCM-4)

The Counter Module (RCM-4) accumulates serial input pulses in four independent counter channels and upon command, the accumulated count is transferred to the parallel PCM data bus. The RCM-4 consists of four independent nine bit binary counters, each with its own set of data transfer gates connected to the parallel PCM data bus, and a programmable address decoder that controls the input gating and data transferring operations for each of the counters. A jumper for optional counter reset is provided. (See Figures 17 and 18.)

Each of the nine bit counters are preceded by an inhibit gate which disables the serial input pulses from being accumulated for a half bit period (2.5 microseconds) at the beginning of the mainframe channel boundry during which the data is transferred to the parallel PCM data bus. However, if an input pulse is received during the input pulse inhibit period, it will be "captured" in a one bit memory and automatically entered into the counter immediately following this period.

The data contained in the selected nine bit counter is transferred to the parallel PCM data bus 1.25 microseconds (one fourth bit period) after the mainframe channel boundary. The

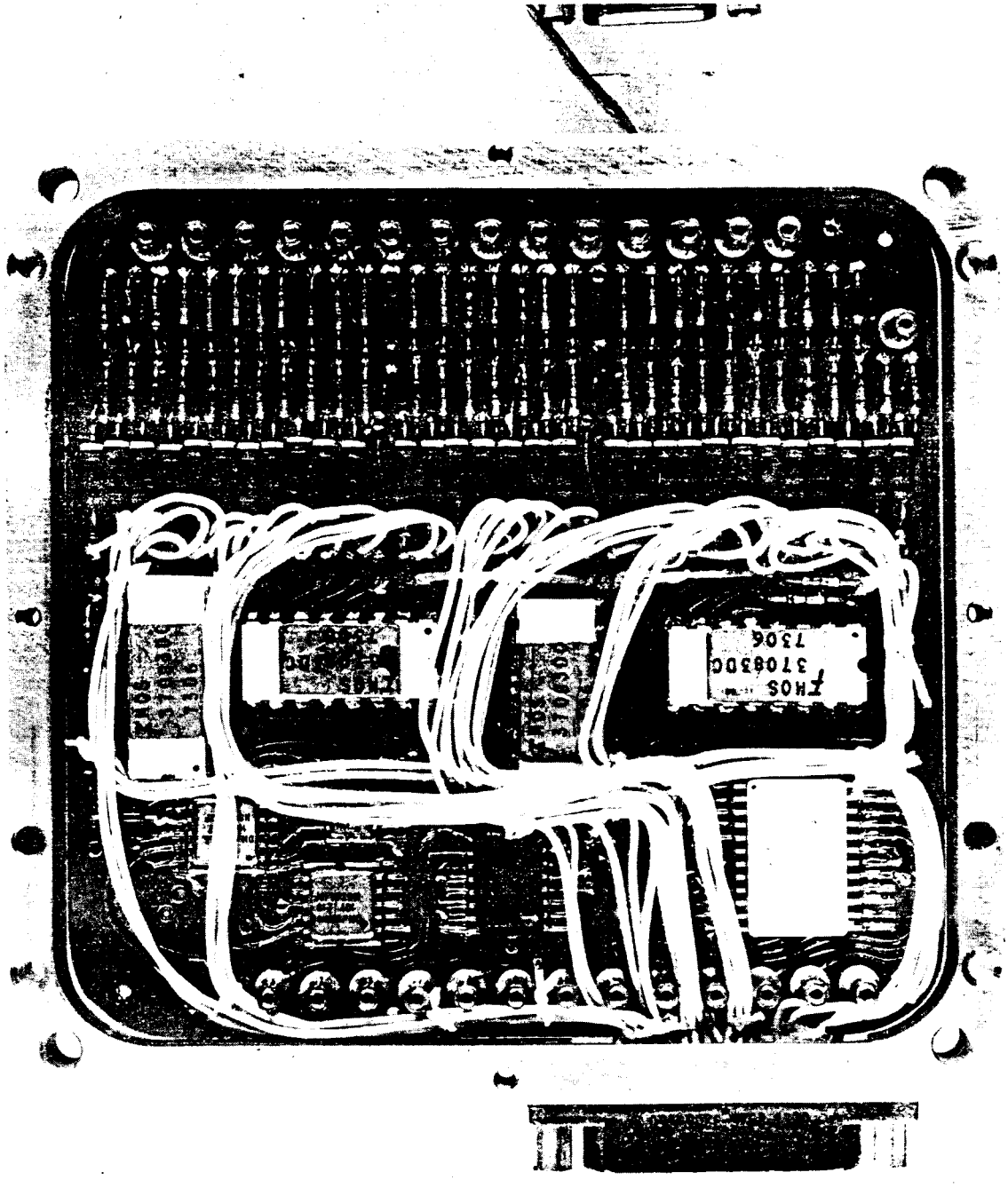


Figure 15a. Analog submultiplexer with calibration and bi-level monitor (ASC-32), top board.

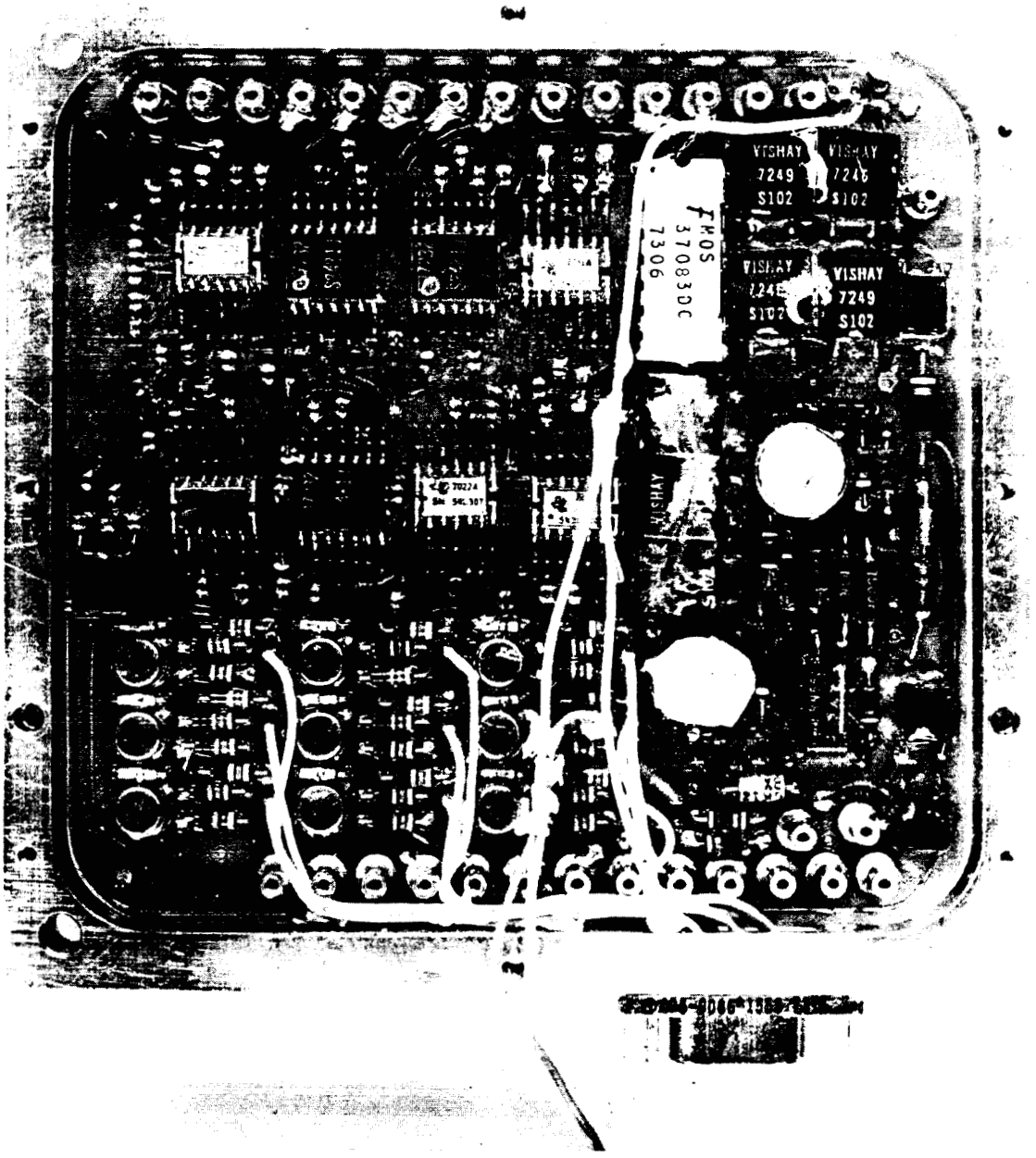


Figure 15b. Analog submultiplexer with calibration and bi-level monitor (ASC-32), bottom board.

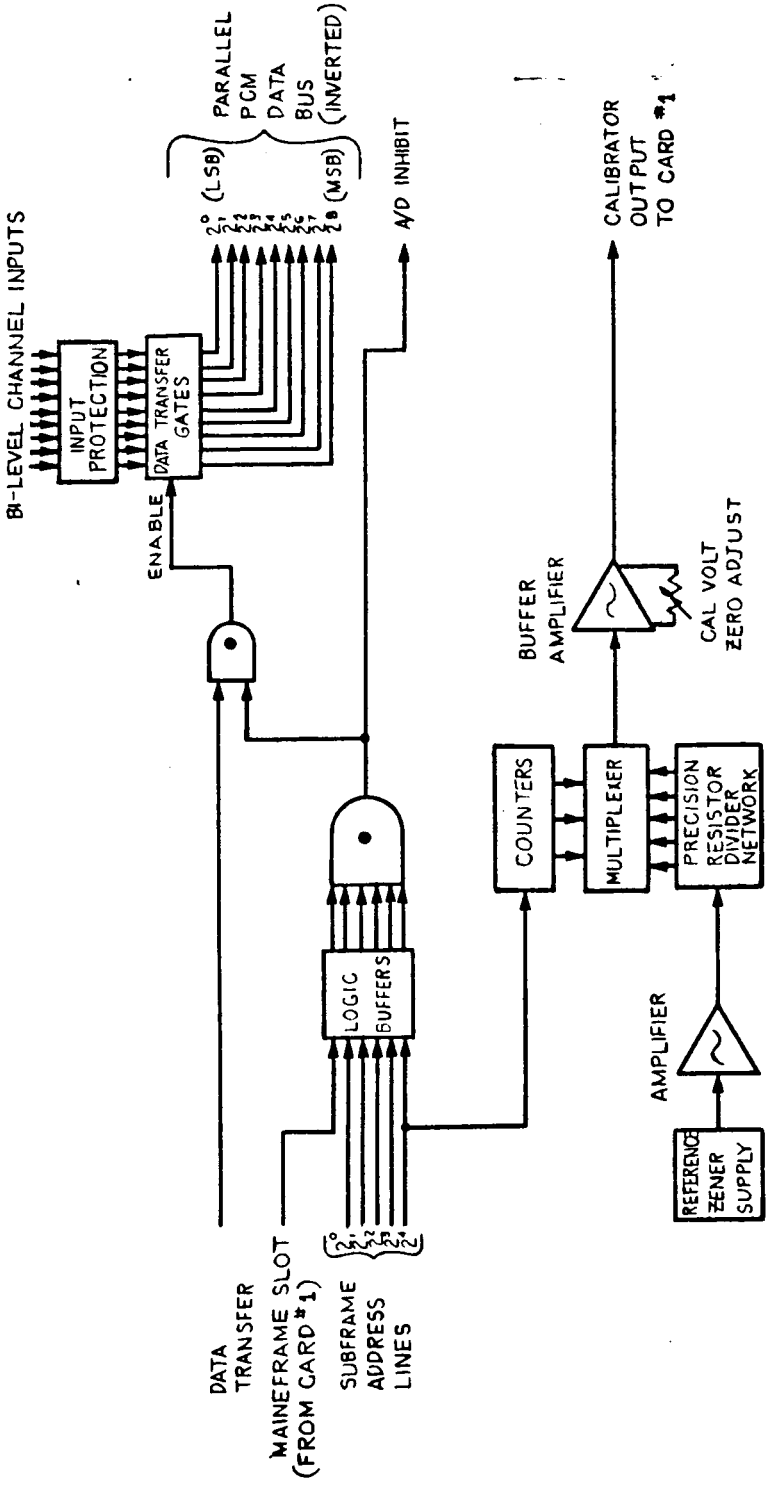


Figure 16. Calibration and bi-level monitor block diagram (card 2 of ASC-32).

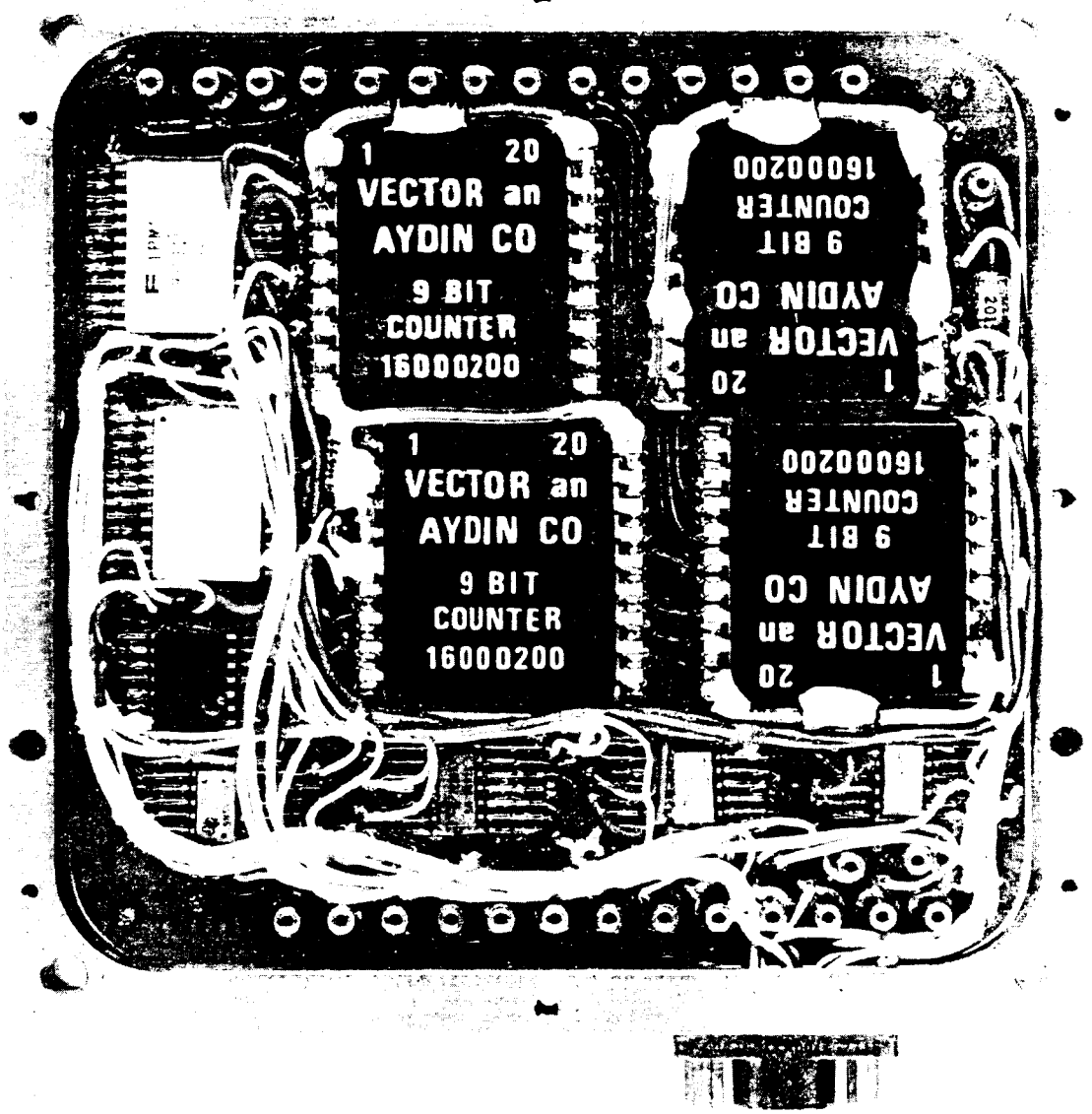


Figure 17. Counter module (RCM–4).

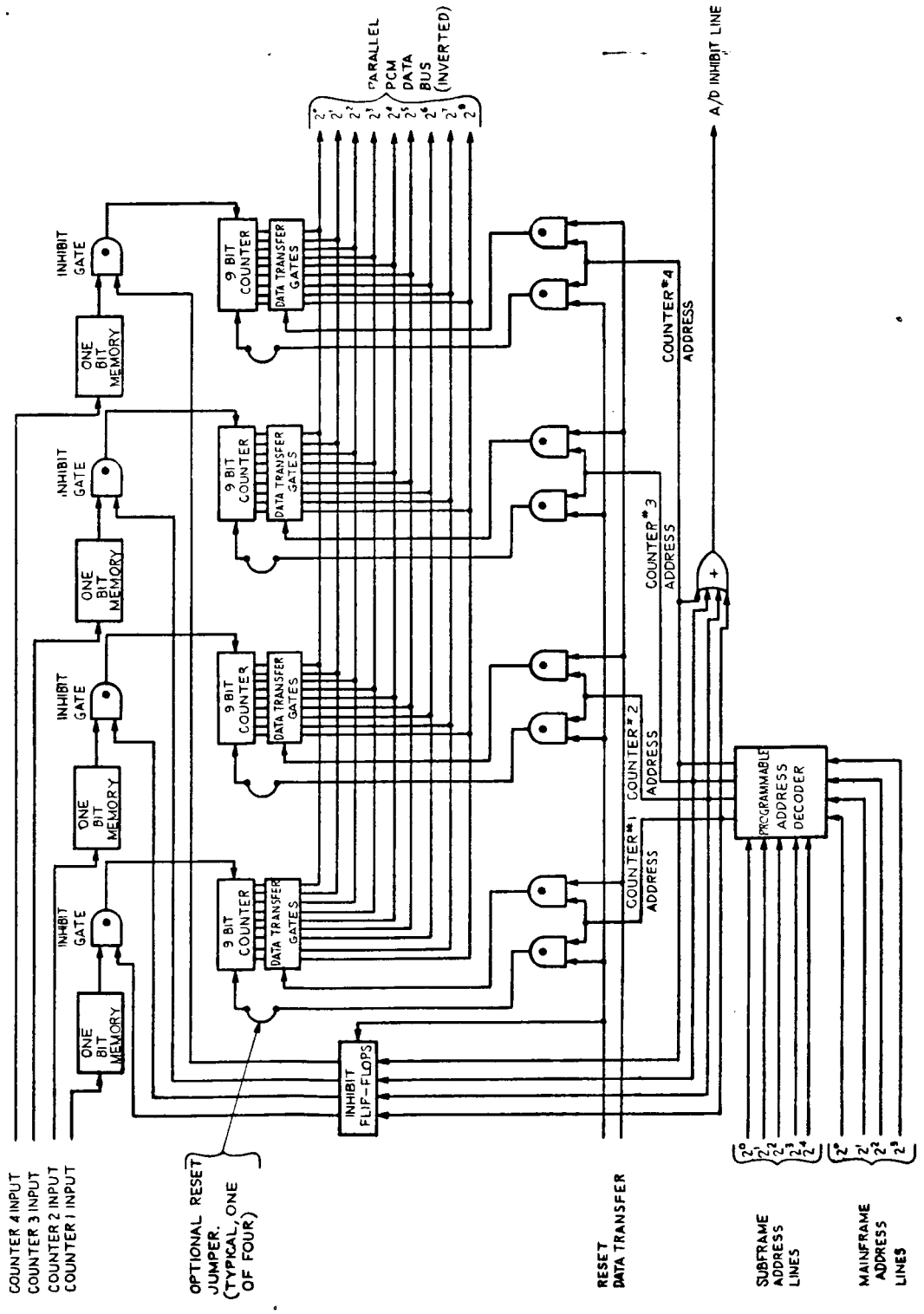


Figure 18. Counter module block diagram.

1.25 microseconds delay between the initiation of the inhibiting of input pulses into the counter and the transferring of the data, provides sufficient time for any count to propagate through the counter and for the data to be stable at the transfer time. Following the data transfer the selected counter will be reset if this option is desired.

Each 9-bit counter overflows after 511 input pulses have been accumulated and will continue to accept input pulses if overflow occurs. During the mainframe channel readout period for each counter, the A/D converter in the encoder is disabled by the A/D inhibit line generated within the programmable address decoder logic.

Serial Input Data Loader Module (SIDL-8)

The Serial Input Data Loader (SIDL-8) accepts nine bit serial input data words into four independent register channels and upon command, transfers the data to the parallel PCM data bus. The SIDL-8 consists of four independent serial to parallel data conversion registers, each with its own set of data transfer gates, and a programmable address decoder that controls the input data gating and data transferring operations for each of the registers. The module also provides an external channel gate signal for each register channel and a data shift clock. (See Figures 19, 20 and 21.)

The channel gate signal is used to enable an external serial data source for shifting its information into the selected nine bit register with the 200 KHz data shift clock that is provided. The selected nine bit serial word is shifted into the register during the mainframe channel preceding its actual location in the PCM format. Each of the nine bit serial data registers are designed so that they are able to accept input data on a continuous basis. If serial data is being supplied on a continuous basis, only the nine bits of data bracketed by the selected channel gate signal will be transferred to the parallel PCM data bus. (The detailed timing relationships between the gate signal and the data shift clock are given in Appendix C.)

The four registers are not reset after the data has been transferred since the new serial information will automatically replace any old data contained in the registers. The reset command from the encoder is used, however, in order to provide a delayed address gate signal. The delayed address gate and the data transfer command enable the data transfer gates so that the register information is loaded into the encoder format in proper sequence. The A/D converter in the encoder is disabled at the proper time by the delayed channel gate from each register which forms the A/D inhibit line.

Signal Buffer (BUF-4)

The Signal Buffer (BUF-4) allows the experimenter access to a number of internal encoder timing signals. (See Figures 22 and 23.) These signals can be used for synchronization, timing, submultiplexing, etc. Each signal is buffered so that the operation of the encoder will not be jeopardized by an accidental short. Two auxiliary inverters are also provided.

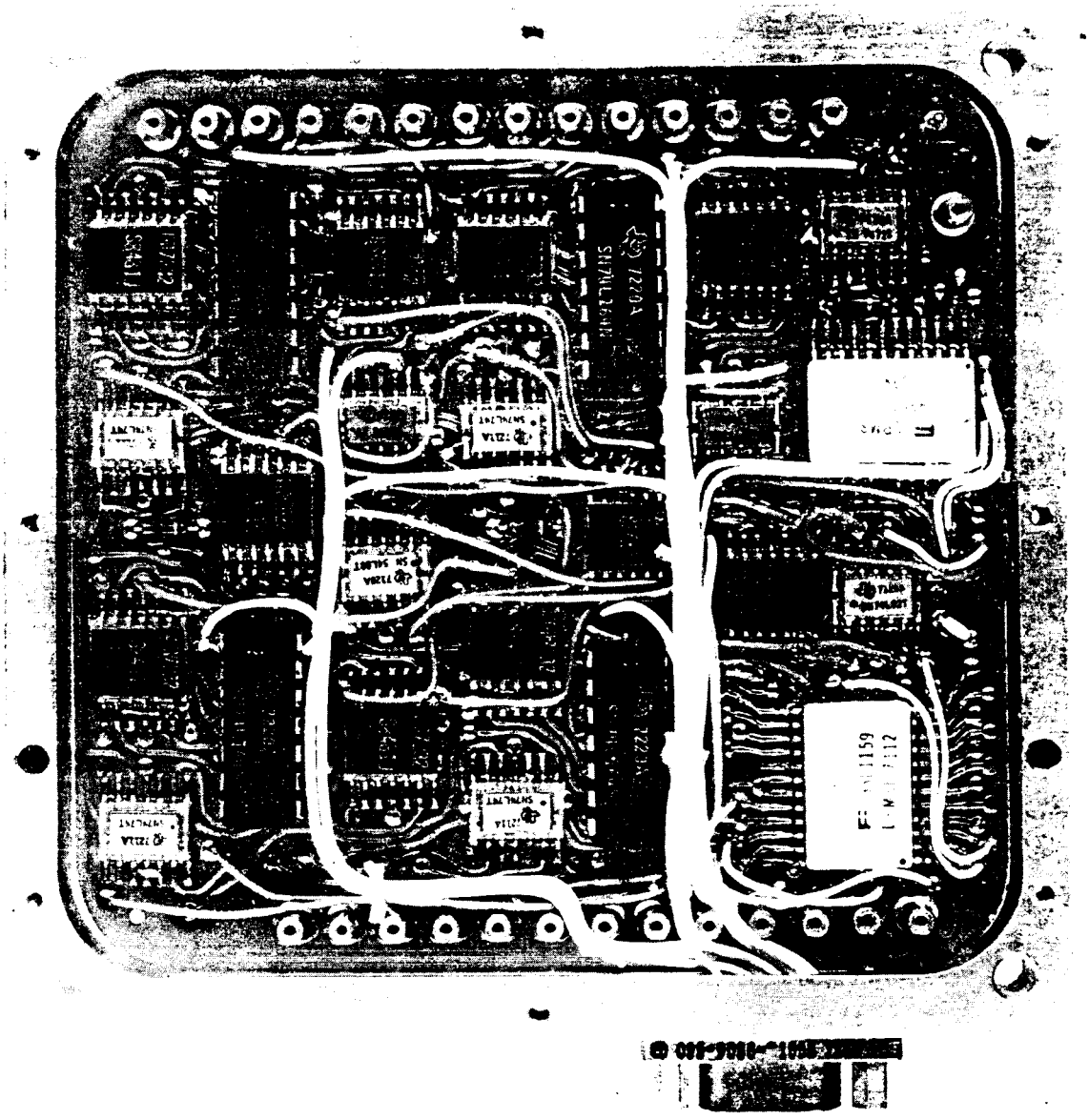


Figure 19. Serial input data loader (SIDL–8).

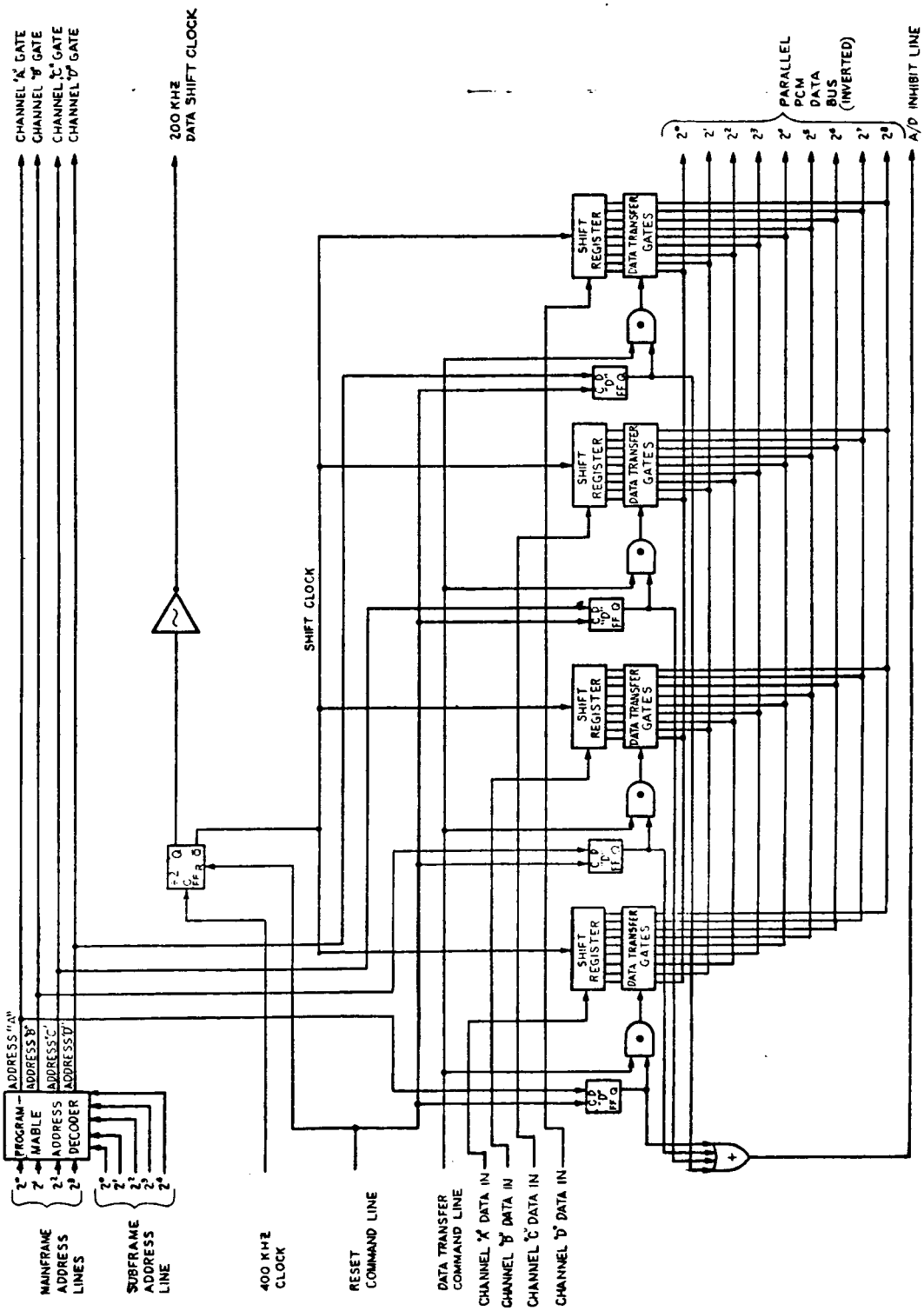


Figure 20. Serial input data loader block diagram.

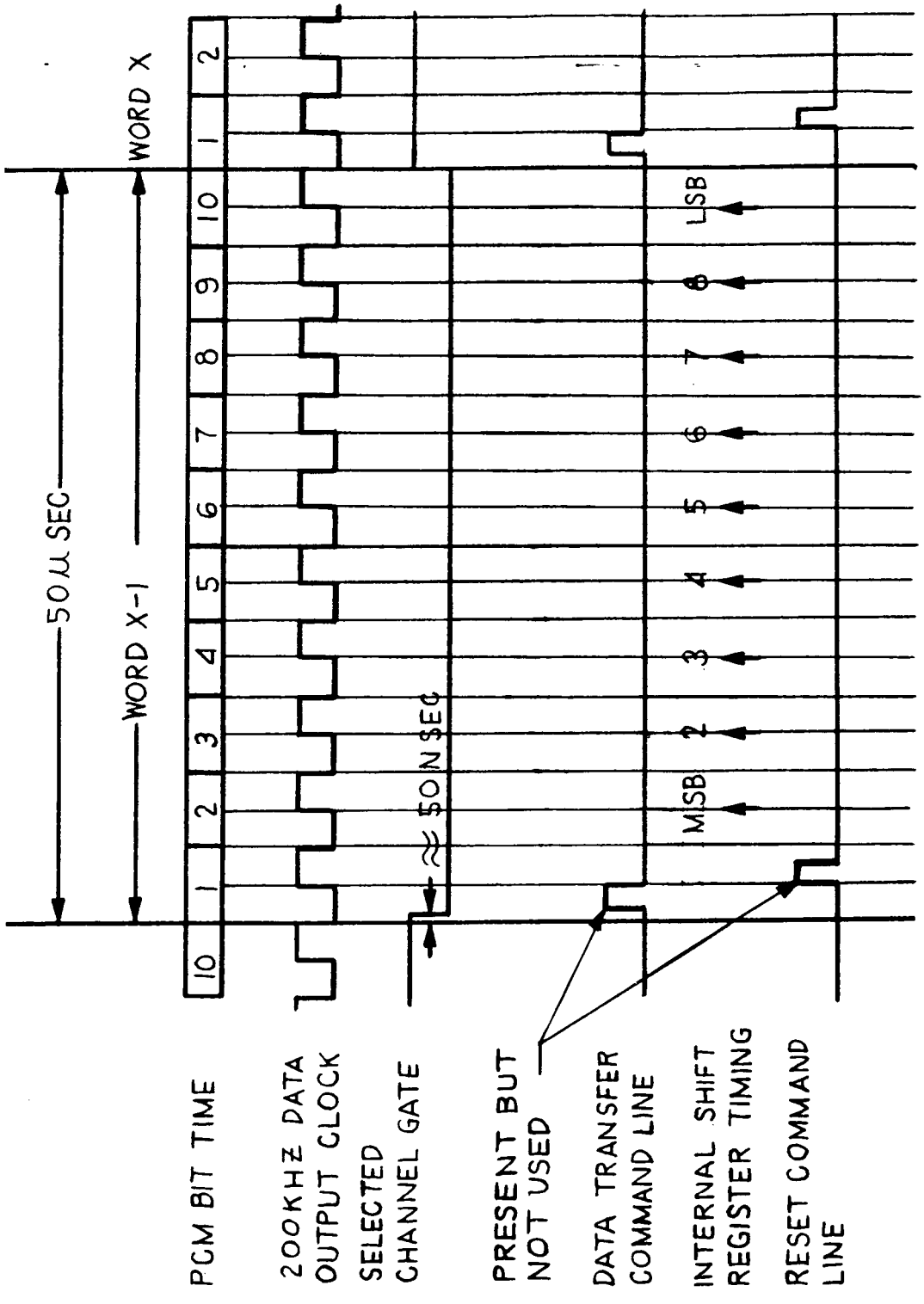


Figure 21. Serial input data loader timing diagram.

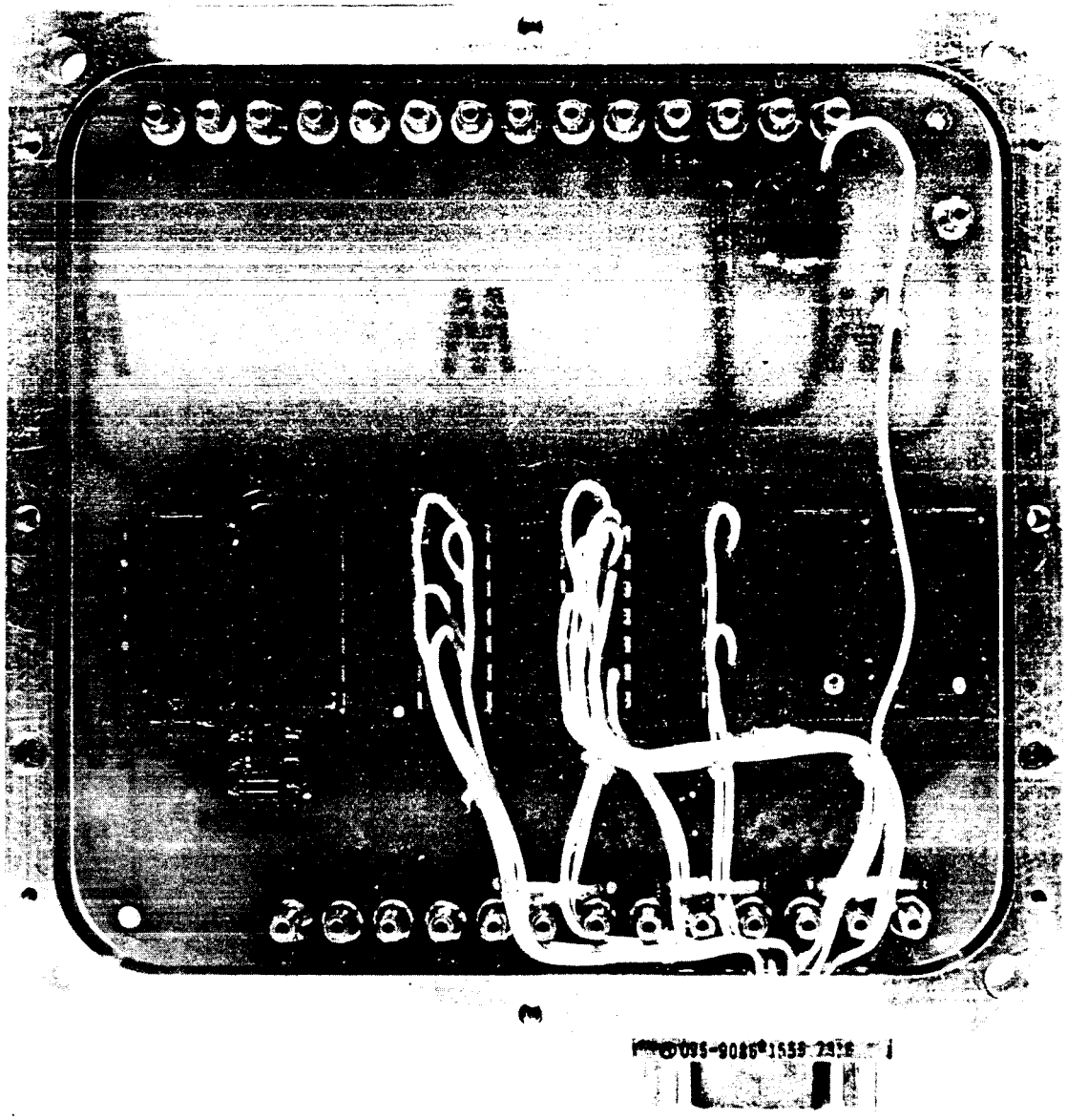


Figure 22. Signal buffer (BUF–4).

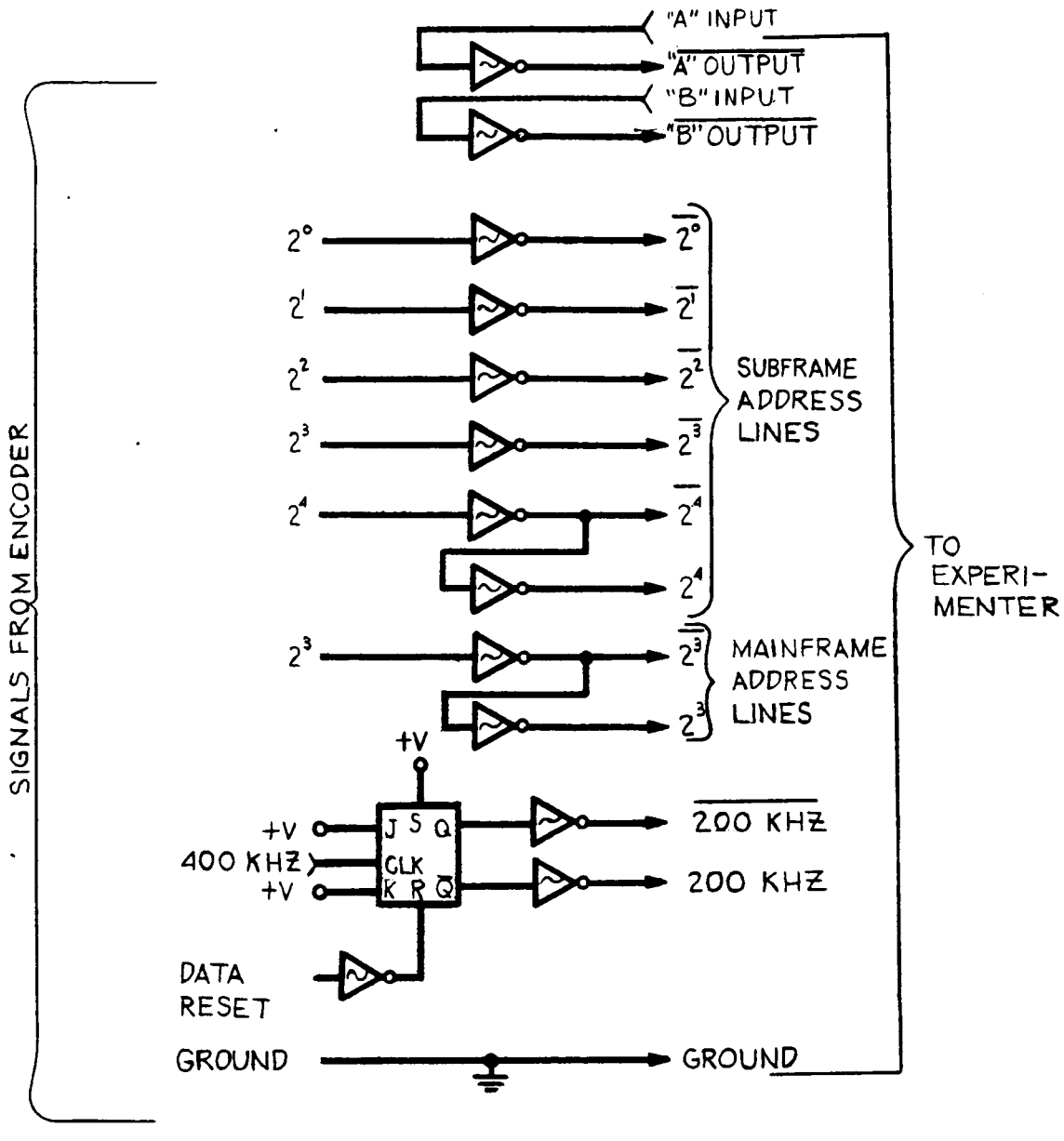


Figure 23. Signal buffer block diagram.

Booster Power Supply (BPS-5)

The Booster Power Supply (BPS-5) augments the mainframe power supply when a large number of expansion modules are used. (See Figures 24 and 25.) The majority of expansion modules use only the +5 volt supply, thus the BPS-5 generates only +5 volt. Its operation is similar to the mainframe supply with two exceptions. A reverse polarity diode is used on the +28 volt input line and the synchronous chopper directly uses the 10 KHz clock.

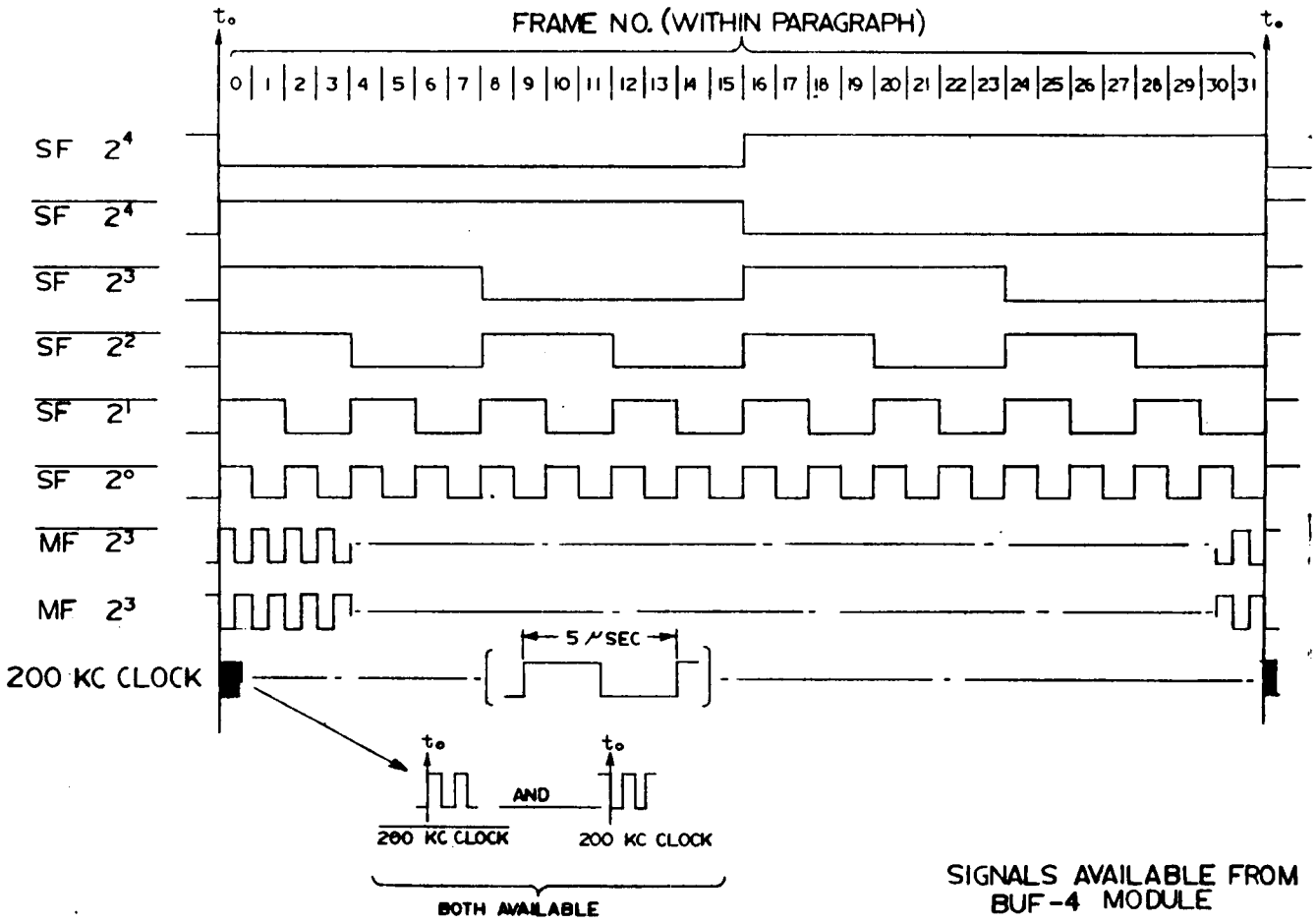


Figure 23A. Signal buffer timing diagram.

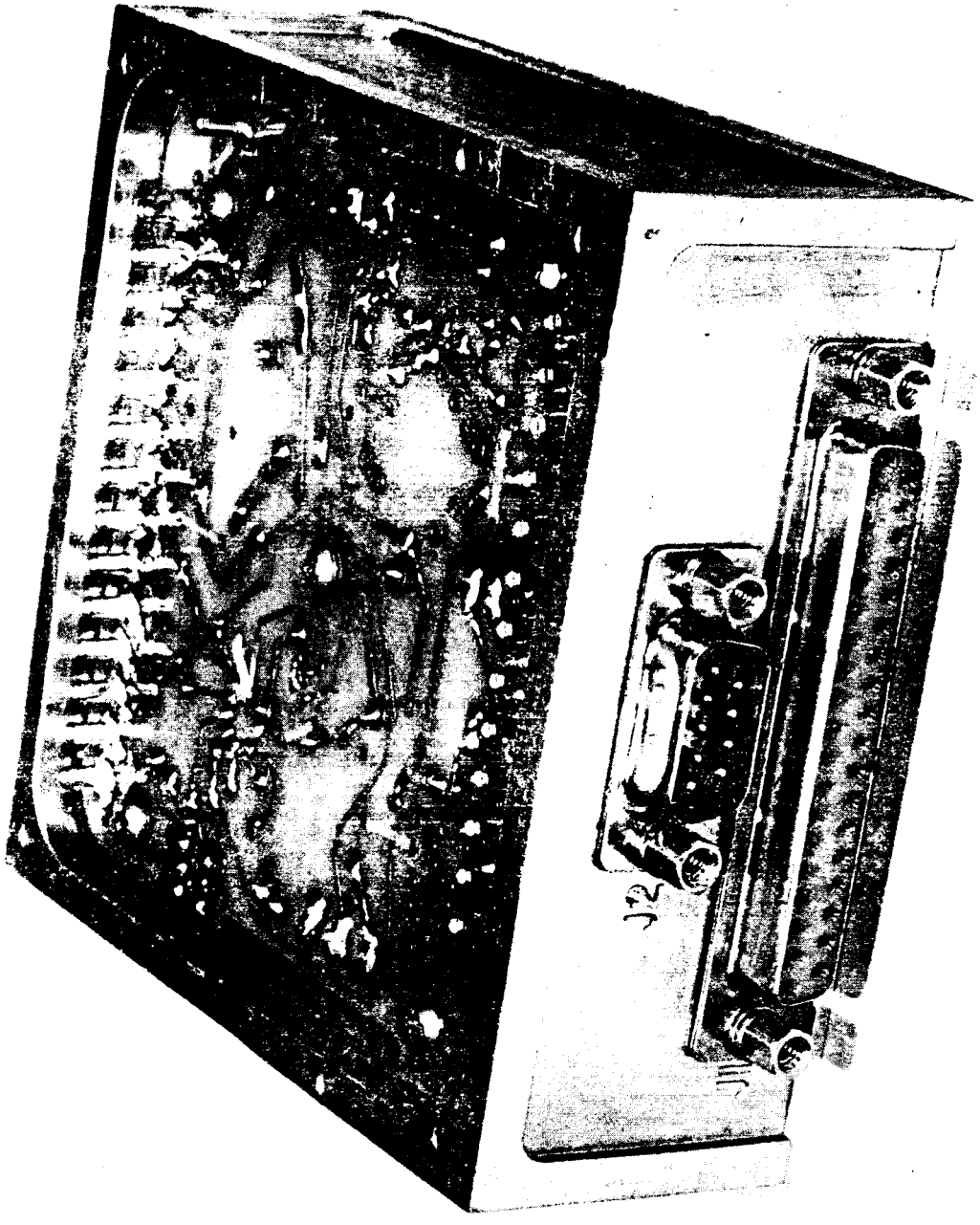


Figure 24. Booster power supply (BPS–5).

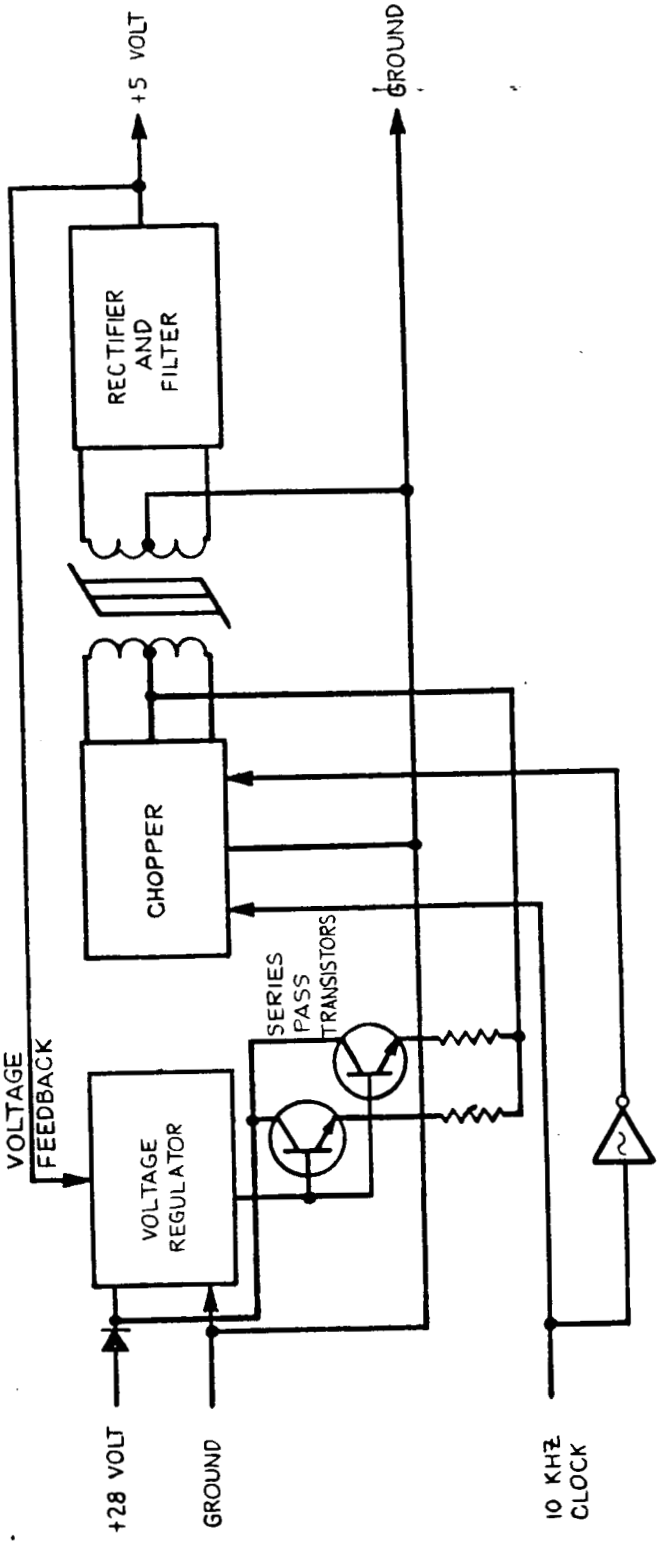


Figure 25. Booster power supply block diagram.

PACKAGING

The mainframe encoder is contained in a milled aluminum case measuring approximately 9.5 centimeters by 9.5 centimeters by 5.5 centimeters high. The expansion modules have the same cross-section as the mainframe encoder and are approximately 0.65 or 1.3 centimeters high. The booster power supply is 3.6 centimeters high.

A typical encoder configuration is shown in Figure 26. Expansion modules are stacked on top of the main encoder until size or power (see Appendix A) limitations are reached. If more modules are required, a second stack is started on top of a booster power supply. An adapter module provides an interface between the main stack and the additional stack.

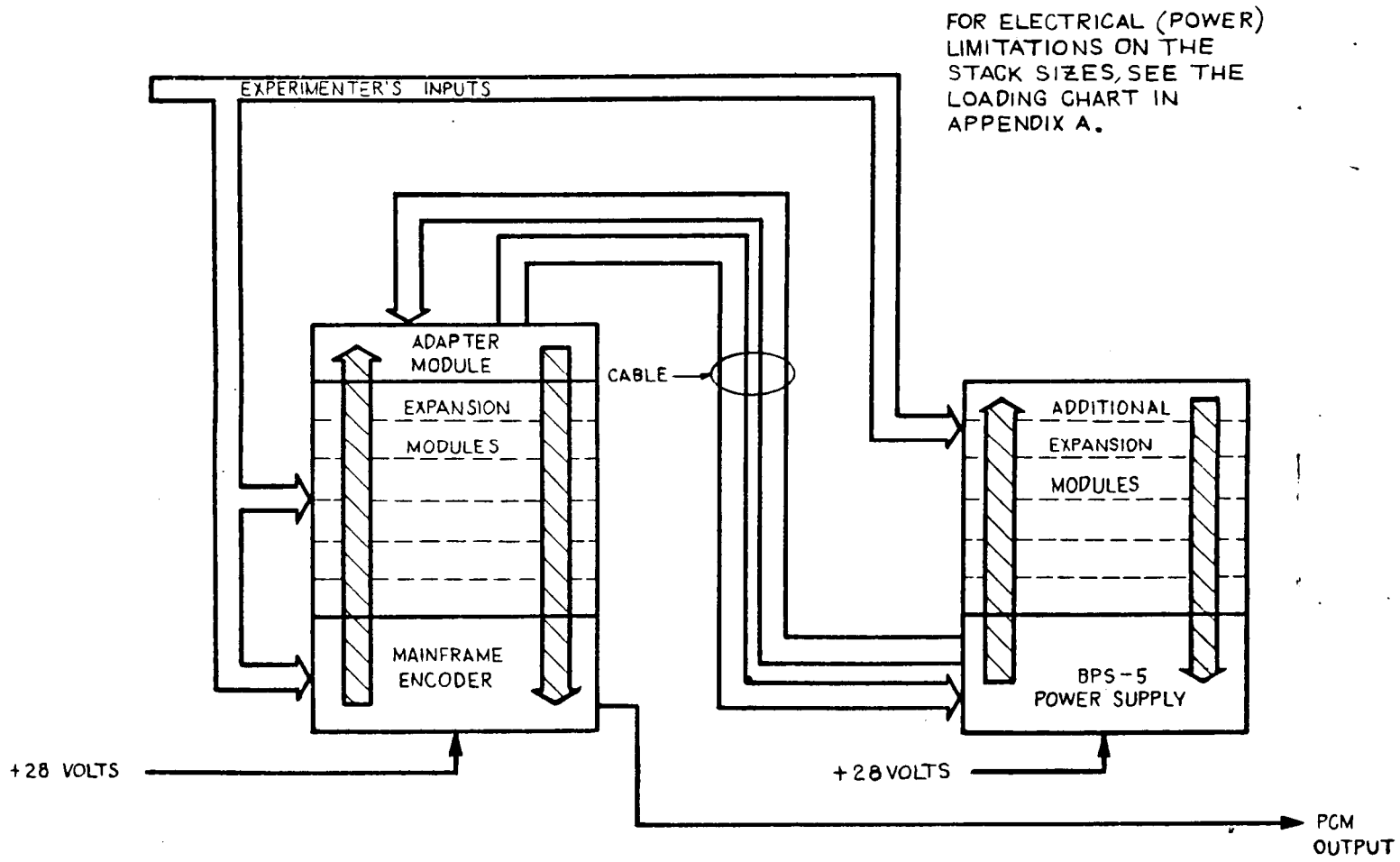


Figure 26. Packaging diagram.

APPENDIX A

SUMMARY OF CONFIGURATIONS

GENERAL

The PCM system can be configured using (1) only the mainframe encoder, (2) expansion modules that are programmed only by their internal programmable address decoders, or (3) expansion modules addressed by the programmable converter (PAC-8). If a large number of expansion modules are used, the mainframe power supply output is augmented by a booster power supply (BPS-5). This appendix will describe (1) the programmable address decoder and its nomenclature, (2) a sample format, (3) when the programmable address converter should be used, and (4) when the booster power supply must be used.

PROGRAMMABLE ADDRESS DECODER

The Programmable Address Decoder (Figure 27) uses a jumper arrangement at the inputs and outputs of two 1-of-16 decoders to decode the desired address for selecting the four digital circuits in an expansion module (the analog address decoder is discussed in the AS-32 section). When both inputs to the AND gates are true, the appropriate circuit is selected and an A/D inhibit signal is generated to allow the digital data to override the analog data (see priority section for further details).

The nomenclature used to identify a specific programming configuration consists of three numbers for each circuit: N_1-N_2-N_3. N_1 designates the mainframe, N_2 designates the first subframe in which the circuit will be selected, and N_3 designates the subcom degree. The subcom degree is 1 of 2^{N_3}. For instance, a circuit designated 3-0-2 would be selected in mainframe 3 during subframes 0, 4, 8, 12, 16, 20, 24, and 28. A circuit designated 15-2-3 would be selected in mainframe 15 during subframes 2, 10, 18, and 26.

Figure 28 illustrates some commonly used jumper configurations. In Part A, the EE jumper determines the N_1 number for all four circuits. If jumper EE-C4 is used, $N_1 = 4$. N_2 and N_3 are determined by the remaining jumpers. The first configuration (jumper K-H and L-J) would result in a module with the following circuit designations: N_1-0-2, N_1-1-2-2, and N_1-3-2. The last configuration of Part A (jumper M-H and N-J) would result in circuit 0 data appearing in subframes 12 and 28 (N_1-12-4), circuit 1 data appearing in subframes 13 and 29 (N_1-13-4), etc. In Part B, one circuit is multiplexed into an entire mainframe. If circuit one is to appear in mainframe 14, jumper AA-C14 would be connected resulting in a 14-0-0 designation. The remaining three circuits can be multiplexed into different mainframes or not used at all. Part C shows how each circuit can be supercommutated to the same degree. If jumper BB-C2 was connected in the first configuration (Y-W), channel 2 would appear in mainframes 2 and 10 (designation 2-0-0 and 10-0-0) or sometimes designated as 2,10-0-0.

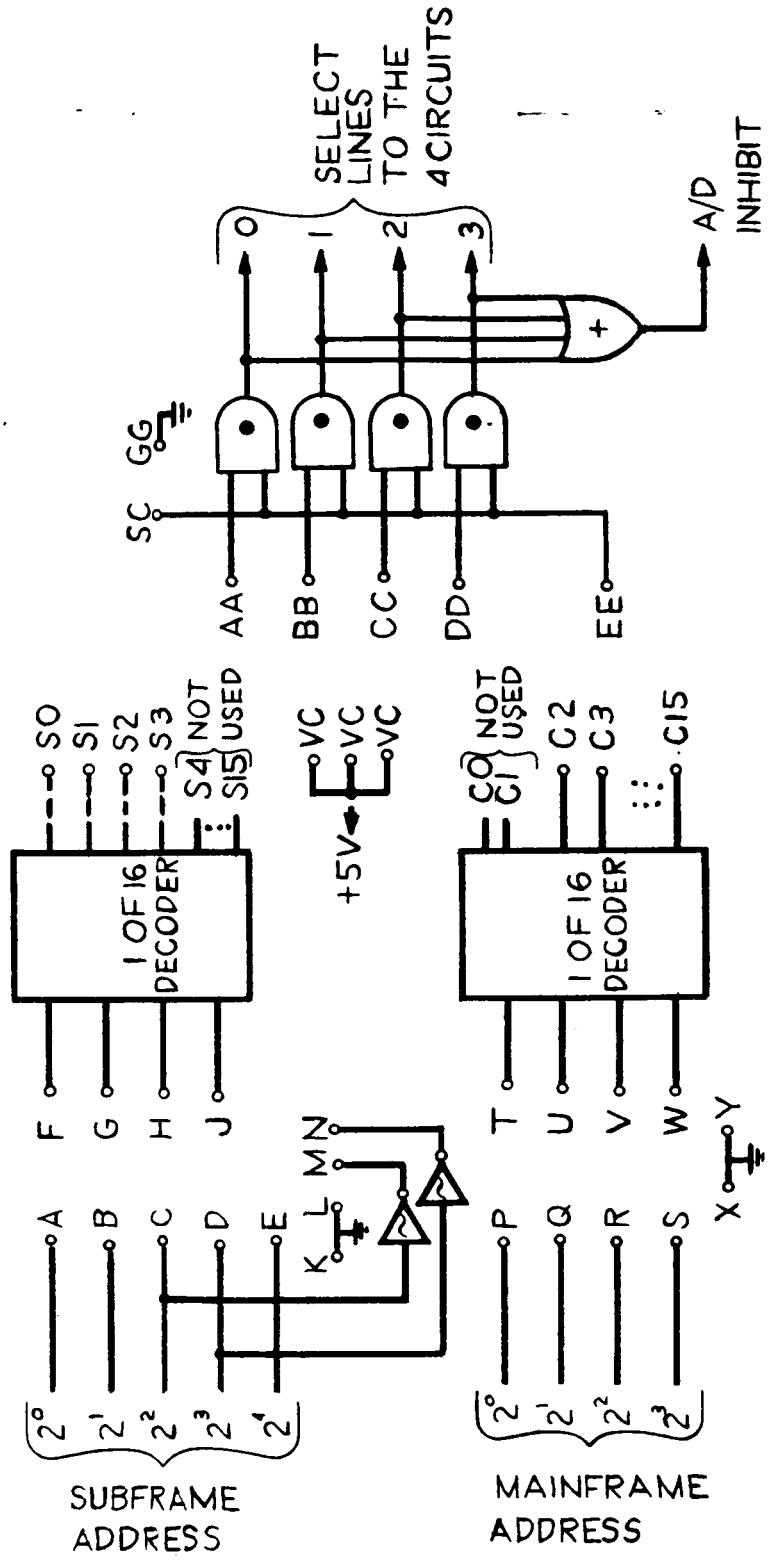


Figure 27. Programmable address decoder.

A. Subcommutation

In all cases, jumper

P–T	S0–AA	A–F
Q–U	S1–BB	B–G
R–V	S2–CC	And EE to the desired channel
S–W	S3–DD	(C2–C15)

Also jumper as required

Submultiplex Channels	Jumper	Module Number	Total Number of Subchannels
0,1,2,3	K–H L–J	0	4
0,1,2,3	C–H L–J	0	8
4,5,6,7	M–H L–J	1	
0,1,2,3	C–H D–J	0	16
4,5,6,7	M–H D–J	1	
8,9,10,11	C–H N–J	2	
12,13,14,15	M–H N–J	3	

B. Mainframe Programming

P–T AA, BB, CC, and DD to the selected mainframe channels

Q–U (C2–C15)

R–V

Figure 28. Programmable address decoder programming table (sheet 1 of 2).

S–W GG–SC All other jumbers can be ignored If less than four units are desired, disable the unwanted channels by connecting AA, BB, CC, or DD to VC.
C. Supercommutation Jumper as in B above except as follows: 2 mainframes per input, Y–W 4 mainframes per input, Y–W, X–V 8 mainframes per input Y–W, X–V, X–U

Figure 28. Programmable address decoder programming table (sheet 2 of 2).

A SAMPLE DATA FORMAT

Figures 29, 30 and 31 illustrate three ways of depicting the same sample format. In all three figures, the following input identifiers are used:

S = Serial Data

A = Analog Data

C = Count Data

D = Parallel Data

CAL = Internal Calibration Data

A channel allocation table (Figure 29) is generated for all formats. For example, the designation 5–0–3 (the designations are fully explained in the previous section) indicates that count input #1 appears in mainframe channel 5 during subframes 0, 8, 16 and 24.

A data matrix (Figure 30) is generated in addition to a channel allocation table for complex formats to aid the user. The matrix is read from left to right and down like a book.

The signal allocation table (Figure 31) is a cross reference list for the data matrix. It presents the same information from a signal input reference.

Channel	Signal Name	Description and/or Comments
0–0–0	sync	
1–0–0	sync & subframe count	
2–0–0	S1	(supercommutated with 10–0–0)
3–0–0	S2	(supercommutated with 11–0–0)
4–0–0	A1	(supercommutated with 12–0–0)
5–0–3	C1	
5–1–3	C2	
5–2–3	C3	
5–3–3	C4	
5–4–3	C5	
5–5–3	C6	
5–6–3	C7	
5–7–3	C8	
6–0–2	C9	
6–1–2	C10	
6–2–2	C11	NOTE: In an actual channel allocation chart, this column would be full.
6–3–2	C12	
7–0–1	C13	
7–1–1	C14	
8–0–2	A2	
8–1–2	A3	
8–2–3	A4	
8–6–3	A5	
8–3–5	A6	
8–7–5	A7	
8–14–5	A8	
8–15–5	A9	
8–19–5	A10	
8–23–5	A11	
8–27–5	A12	
8–31–5	A13	
9–0–5	A14	
9–1–5	A15	
↓	↓	
9–31–5	A45	

Figure 29. Channel allocation table (sheet 1 of 2).

Channel	Signal Name	Description and/or Comments
10-0-0	See 2-0-0	
11-0-0	See 3-0-0	
12-0-0	See 4-0-0	
13-0-0	A46	
14-0-4	A47	
14-1-4	A48	
14-2-4	A49	
14-3-5	A50	
14-4-5	A51	
↓	↓	
14-15-5	A62	
14-19-5	A63	
14-20-5	A64	
↓	↓	
14-31-5	A75	
15-0-5	D1	(9 bit parallel binary)
15-1-5	A76	
15-2-5	C15	
15-3-5	A77	
15-4-3	S3	
15-5-5	A78	
15-6-5	A79	
↓	↓	
15-11-5	A84	
15-13-5	A85	
15-14-5	A86	
15-15-5	A87	
15-16-5	A88	
15-17-5	A89	
15-18-5	C16	
15-19-5	A90	
15-21-5	A91	
15-22-5	A92	
15-23-5	A93	
15-24-5	A94	
15-25-5	A95	
15-26-5	A96	
15-27-5	A97	
15-29-5	A99	
15-30-5	A99	
15-31-5	CAL	(internal calibrator)

Figure 29. Channel allocation table (sheet 2 of 2).

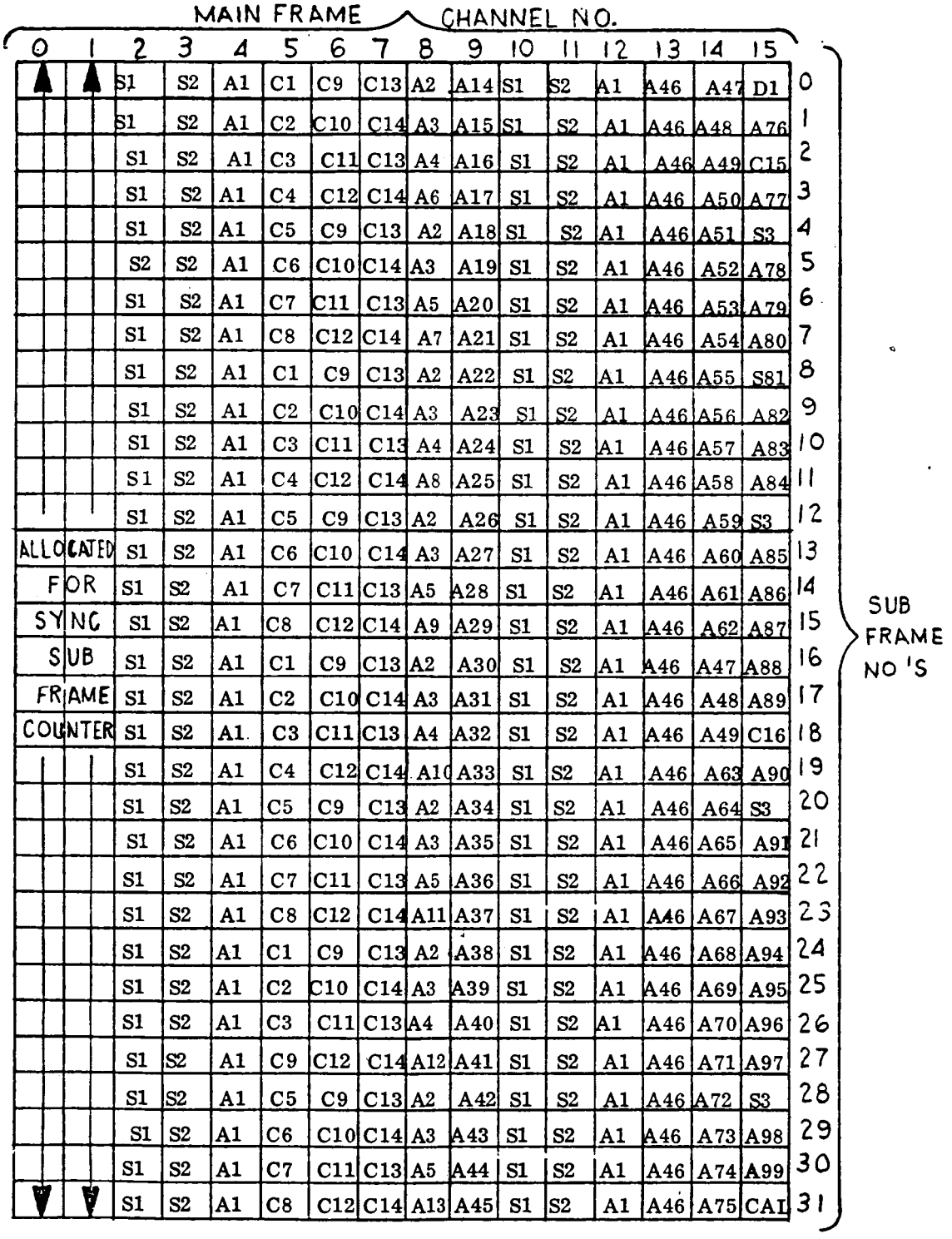


Figure 30. Sample data matrix.

Signal Name	Program Designation	Samples Per Second	Comments
S1	2, 10–0–0	2500	supercommutated
S2	3, 11–0–0	2500	supercommutated
S3	15–4–3	160	
D1	15–0–5	40	9 bit parallel binary input
CAL	15–31–5	40	internal calibrator (5v, 4v, 3v, 2v, 1v, 0v, 0v, 0v)
C1	5–0–3	160	
C2	5–1–3	160	
C3	5–2–3	160	
C4	5–3–3	160	
C5	5–4–3	160	
C6	5–5–3	160	
C7	5–6–3	160	
C8	5–7–3	160	
C9	5–0–2	320	
C10	6–1–2	320	
C11	6–2–2	320	
C12	6–3–2	320	
C13	7–0–1	640	
C14	7–1–1	640	
C15	15–2–5	40	
C16	15–18–5	40	
A1	4, 12–0–0	2500	
A2	8–0–2	320	
A3	8–1–2	320	
A4	8–2–3	160	
A5	8–6–3	160	
A6	8–3–5	40	
A7	8–7–5	40	
A8	8–11–5	40	
A9	8–15–5	40	
A10	8–19–5	40	
A11	8–23–5	40	
A12	8–27–5	40	

Figure 31. Signal allocation table (sheet 1 of 2).

Signal Name	Program Designation	Samples Per Second	Comments
A13	8-31-5	40	
A14	9-0-5	40	
↓	↓	↓	
A45	9-31-5	40	
A46	13-0-0	1250	
A47	14-0-4	80	
A48	14-1-4	80	
A49	14-2-4	80	
A50	14-3-5	40	
↓	↓	↓	
A62	14-15-5	40	
A63	14-19-5	40	
↓	↓	↓	
A75	14-31-5	40	
A76	15-1-5	40	
A77	15-3-5	40	
A78	15-5-5	40	NOTE: In an actual allocation table, this column would be filled in.
A79	15-6-5	40	
A80	15-7-5	40	
A81	15-8-5	40	
A82	15-9-5	40	
A83	15-10-5	40	
A84	15-11-5	40	
A85	15-13-5	40	
A86	15-14-5	40	
A87	15-15-5	40	
A88	15-16-5	40	
A89	15-17-5	40	
A90	15-19-5	40	
A91	15-21-5	40	
A92	15-22-5	40	
A93	15-23-5	40	
A94	15-24-5	40	
A95	15-25-5	40	
A96	15-26-5	40	
A97	15-23-5	40	
A98	15-29-5	40	
A99	15-30-5	40	

Figure 31. Signal allocation table (sheet 2 of 2).

PROGRAMMABLE ADDRESS CONVERTER (PAC-8)

The PAC-8 module is used when either the required format cannot be generated by using the current stock of programmed modules, or format changes are anticipated. As discussed in the PAC-8 section of this document, the entire format can be changed in a few hours with no rewiring if the PAC-8 module is used.

BOOSTER POWER SUPPLY (BPS-5)

Expansion modules are stacked on top of the mainframe encoder until physical or electrical limits are reached. When these limits are reached, a new stack is started on top of a booster power supply. The mainframe stack is interconnected to the BPS-5 stack through an adapter module and cable assembly (see packaging section). The physical limit of the mainframe stack is governed by the particular experiment packaging and the electrical limit is governed by the +5 volt current drain. The mainframe power supply's residual +5 volt current that is available for the expansion modules is 400 milliampere. The BPS-5 can supply +5 volt @ 1.25 ampere. The +5 volt current drain of the modules is as follows:

Adapter module: 160 ma

Programmable Address Converter (PAC-8): 70 ma

Analog Submultiplexer (AS-32): 80 ma

Analog Submultiplexer with Calibration and Bi-Level Monitor (ASC-32): 100 ma

Counter Module (RCM-4): 200 ma

Serial Input Data Loader (SIDL-8): 200 ma

Signal Buffer (BUF-4): 45 ma

LOADING CHART

The mainframe will drive 8 normalized loads and the booster power supply (BPS-5) will drive 25 normalized loads. The normalized loads of the submodules are as follows:

AS-32	1.5
ASC-32	2
RCM-4	4
SIDL-8	4
BUF-4	1
PAC-8	1.5

APPENDIX B

SUMMARY OF SPECIFICATIONS

1. Mainframe Encoder

Output Bit Rate:	200 kilobits/second
Word Rate:	20 kilowords/second (MSB first, parity last)
Mainframe:	2 sync words plus 14 data words
Subframe:	32 subframes per mainframe
Parity:	Odd
Word:	9 data bits plus parity bit
Output Code:	Bi-Ø-L
Output Voltage:	"1" = positive transition "0" = negative transition
Analog Input Voltage Range:	-0.1 to +5.1 volts
Analog Input Protection:	To ±30 volts
Analog Input DC Impedance:	1 megohm
Analog Input Maximum Source Impedance:	5.6 kilohm (see Appendix C)
Power Input:	+26 to +34 volts DC @ 250 milliamperes
Power Efficiency:	70% @ 32 volt, full load
Residual Power: (For expansion modules)	+5 volt @ 400 milliampere +12 volt @ 70 milliampere -12 volt @ 70 milliampere -27 volt @ 35 milliampers
Length:	9.5 centimeter
Width:	9.5 centimeter
Height:	5.5 centimeter
Weight:	595 grams

2. Programmable Address Decoder (PAC-8)

Memory Size:	256 words x 8 bits
Power Input:	+5 volt @ 70 ma -12 volt @ 10 ma
Height:	1.3 cm
Weight:	150 grams

3. Analog Submultiplexer (AS-32)

Analog Inputs:	32 channels
Analog Input Voltage Range:	-0.1 to +5.1 volts
Analog Input Protection:	To ±30 volts
Analog Input DC Impedance:	1 megohm
Analog Input Maximum Source Impedance:	5.6 kilohms (See Appendix C)
Power Input:	+5 volt @ 80 ma -27 volt @ 25 ma
Height:	0.65 centimeter
Weight:	89 grams

4. Analog Submultiplexer with Calibration and Bi-Level Monitor (ASC-32)

Digital Inputs:	9 bits
Digital Input Logic:	TTL ("0" = 0 volts @ -0.8 ma, "1" = +5 volts @ 0.025 ma
Calibration Levels:	0, 1, 2, 3, 4 and 5 volts
Analog Inputs:	30 channels
Analog Input Voltage Range:	-0.1 to +5.1 volts
Analog Input Protection:	To ±30 volts
Analog Input DC Impedance:	1 megohm
Analog Input Maximum Source Impedance:	5.6 kilohms (See Appendix C)
Power Input:	+5 volt @ 100 ma +12 volt @ 5 ma -12 volt @ 5 ma -27 volt @ 35 ma

Height:	1.3 cm
Weight:	182 grams

5. Counter Module (RCM–4)

Count Inputs:	4 channels, 9 bits each accumulated
Count Input Logic:	Low power TTL (1 unit load)
Power Input:	+5 volt @ 200 ma
Height:	0.65 cm
Weight:	93 grams

6. Serial Input Data Loader (SIDL–8)

Serial Inputs:	Four 9–bit channels
Serial Input Logic:	TTL (2 unit loads)
Channel Gate and Clock Output Logic:	TTL (10 unit loads)
Power Input:	+5 volt @ 200 ma
Height:	0.65 centimeter
Weight:	86 grams

7. Signal Buffer (BUF–4)

Output Logic:	TTL (10 unit loads)
Buffer Input Logic:	TTL (1 unit load)
Power Input:	+5 volt @ 45 ma
Height:	0.65 cm
Weight:	73 grams

8. Booster Power Supply (BPS–5)

Power Input:	+24 to +38 VDC @ 105 milliamperes (nominal)
Power Efficiency:	65% @ 32 VDC, full load
Power Output:	+5 VDC @ 1.25 amperes
Height:	3.6 cm
Weight:	524 grams

APPENDIX C

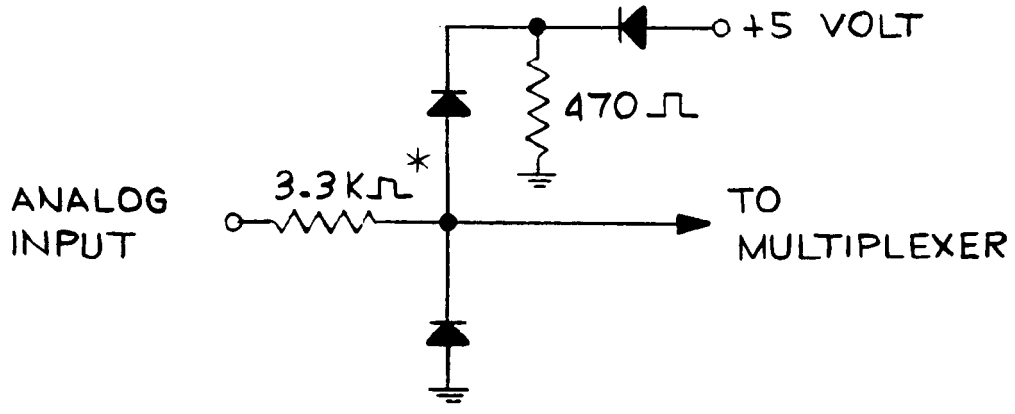
EXPERIMENTER INTERFACE

The experimenter interfaces with the mainframe encoder and all the expansion modules with the exception of the Programmable Address Converter (PAC-8) and Booster Power Supply (BPS-5). The operation of each unit has been described in the functional description section of this document and the specifications have been summarized in Appendix B. This appendix will summarize and expand on only those parts of the system with which the experimenter interfaces.

MAINFRAME ANALOG MULTIPLEXER

The 14 mainframe analog inputs are multiplexed into each of the 14 mainframe data channels (the remaining two mainframe channels are reserved for sync). The inputs are multiplexed and converted (analog to digital) in the mainframe preceding their location in the output format. The inputs cannot be subcommutated; supercommutation can be implemented by tying the appropriate inputs together. The mainframe inputs are automatically overridden by the expansion modules.

The inputs are protected from over and under voltages to ±35 volts by the following input protection circuit:



* 5.6 K for AS-32 and ASC-32 expansion modules.

The recommended maximum source impedance for the analog inputs is 5.6 kilohms, or less. The analog input range is -0.1 to +5.1 volts for valid data. Protection is provided up to ±35 volts. The analog input DC impedance is 1 megohm.

ANALOG SUBMULTIPLEXER (AS-32)

The AS-32 can be internally programmed to subcommutate analog inputs into any of the mainframe data channels. Subcom rates of 2, 4, 8, or 16 can be selected. The subcommutated analog data automatically overrides the mainframe analog data and is overridden by digital data. The timing and input specification are the same as for the mainframe analog multiplexer except that the series input resistor is 5.6 kΩ.

ANALOG SUBMULTIPLEXER WITH CALIBRATION AND BI-LEVEL MONITOR (ASC-32)

The ASC-32 is identical with AS-32 with two exceptions. In subframe 0, a 9-bit bi-level input overrides the analog input. The nine digital inputs must maintain TTL logic levels while sinking 0.8 milliampere at 0 volts (logic "0") and sourcing 0.025 milliampere at +5 VDC (logic "1"). In subframe 31, a calibration input is processed. The calibration input follows the sequence 5 V, 4 V, 3 V, 2 V, 1 V, 0 V, 0 V and 0 volt. Thus there are 30 analog inputs for use by the experimenter.

COUNTER MODULE (RCM-4)

The RCM-4 has four 9-bit counters. These counters can be subcommutated or supercommutated as discussed in the Programmable Address Decoder section of this document. A 1-bit memory allows the counters to be read out at the beginning of the word in which they are outputed without losing a count during the readout time. An optional jumper may be used to reset the counters after readout. The counters automatically override all analog data during their programmed location in the format. The count input interface is a one-unit load, low power TTL interface, which is independent of rise and fall time.

SERIAL INPUT DATA LOADER (SIDL-8)

The SIDL-8 has four 9-bit serial to parallel converter channels. These channels can be subcommutated or supercommutated as discussed in the Programmable address decoder section of this document. A timing diagram of the SIDL-8 is shown in Figure 32. The timing diagram includes the suggested experimenter shift timing. A channel gate for each of the four channels and the 200 KHz data output clock are supplied to the experimenter. Since the shift registers in the module shift during positive clock edges. it is suggested that the experimenter shift on negative edges. Whether the experimenter will need 8 or 9 shift pulses will depend on whether his register is being loaded in serial or parallel. The only data that is meaningful to the SIDL-8 module is the data that appears on the selected channel data input at the 9 positive transitions of the output clock during the selected channel gate time.

Each channel data input line must drive two standard TTL unit loads. The channel gate and clock outputs can each drive ten standard TTL unit loads.

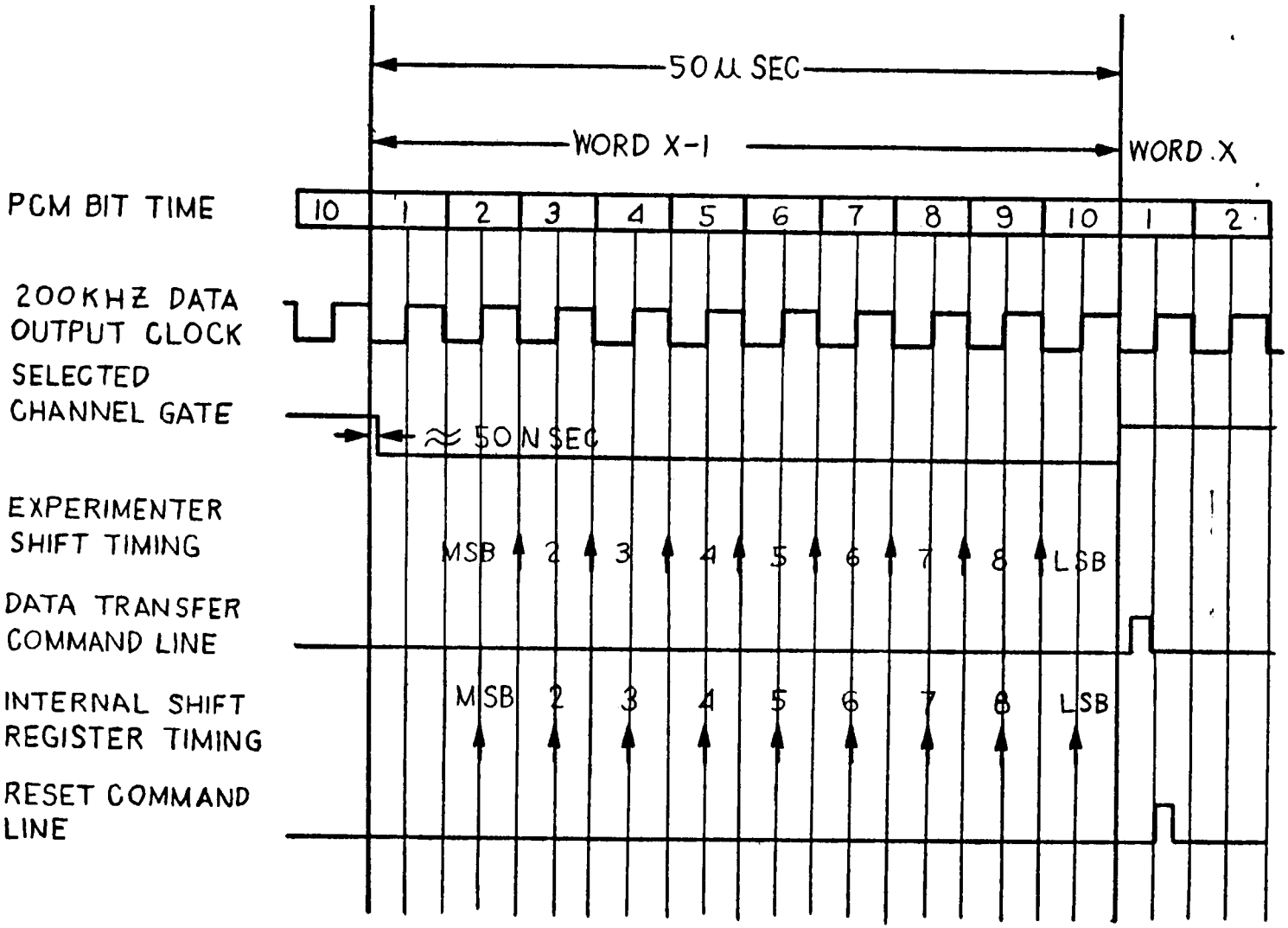


Figure 32. Serial input data loader timing diagram.

APPENDIX D

SUBMODULE PIN CONNECTIONS

BUF-4 CONNECTOR PIN FUNCTIONS

Pin #	Function
1	$\overline{SF\ 2^4}$
2	$SF\ 2^4$
3	$\overline{SF\ 2^3}$
4	$\overline{SF\ 2^2}$
5	$\overline{SF\ 2^1}$
6	$\overline{SF\ 2^0}$
7	$\overline{MF\ 2^3}$
8	$MF\ 2^3$
9	BUFFER A IN
10	BUFFER A OUT
11	BUFFER B IN
12	BUFFER B OUT
13	200 KC
14	$\overline{200\ KC}$
15	Ground

AS-32 CONNECTOR PIN FUNCTIONS

Pin #	Function
1	INPUT #0
2	INPUT #1
3	INPUT #2
4	INPUT #3

Pin #	Function
5	INPUT #4
6	INPUT #5
7	INPUT #6
8	INPUT #7
9	INPUT #8
10	INPUT #9
11	INPUT #10
12	INPUT #11
13	INPUT #12
14	INPUT #13
15	INPUT #14
16	INPUT #15
17	INPUT #16
18	INPUT #17
19	INPUT #18
20	INPUT #19
21	INPUT #20
22	INPUT #21
23	INPUT #22
24	INPUT #23
25	INPUT #24
26	INPUT #25
27	INPUT #26
28	INPUT #27
29	INPUT #28
30	INPUT #29
31	INPUT #30

Pin #	Function
32	INPUT #31
33	not used
34	not used
35	not used
36	not used
37	INPUT GROUND

ASC-32 LARGE CONNECTOR (J1) PIN FUNCTIONS

Pin #	Function
1	not used
2	INPUT #1
3	INPUT #2
4	INPUT #3
5	INPUT #4
6	INPUT #5
7	INPUT #6
8	INPUT #7
9	INPUT #8
10	INPUT #9
11	INPUT #10
12	INPUT #11
13	INPUT #12
14	INPUT #13
15	INPUT #14
16	INPUT #15
17	INPUT #16
18	INPUT #17
19	INPUT #18

Pin #	Function
20	INPUT #19
21	INPUT #20
22	INPUT #21
23	INPUT #22
24	INPUT #23
25	INPUT #24
26	INPUT #25
27	INPUT #26
28	INPUT #27
29	INPUT #28
30	INPUT #29
31	INPUT #30
32	not used
33	not used
34	not used
35	not used
36	not used
37	INPUT GROUND

ASC-32 SMALL CONNECTOR (J2) PIN FUNCTIONS

Pin #	Function
1	BI-LEVEL (2^0 POSITION)
2	BI-LEVEL (2^1 POSITION)
3	BI-LEVEL (2^2 POSITION)
4	BI-LEVEL (2^3 POSITION)
5	BI-LEVEL (2^4 POSITION)
6	BI-LEVEL (2^5 POSITION)
7	BI-LEVEL (2^6 POSITION)

Pin #	Function
8	BI-LEVEL (2^7 POSITION)
9	BI-LEVEL (2^8 POSITION)
10	ground
11	not used
12	not used
13	not used
14	not used
15	not used

SIDL-8 CONNECTOR PIN FUNCTIONS

Pin #	Function
1	INPUT #0
2	ENABLE #0
3	INPUT #1
4	ENABLE #1
5	INPUT #2
6	ENABLE #2
7	INPUT #3
8	ENABLE #3
9	200 KC SHIFT CLOCK
10	not used
11	not used
12	not used
13	not used
14	not used
15	INPUT GROUND

RCM-4 CONNECTOR PIN FUNCTIONS

Pin #	Function
1	INPUT #0
2	INPUT #1
3	INPUT #2
4	INPUT #3
5	MSB OUTPUT #0
6	MSB OUTPUT #1
7	MSB OUTPUT #2
8	MSB OUTPUT #3
9	INPUT GROUND